

Statistical Skew Modeling for General Clock Distribution Networks in Presence of Process Variations

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Abstract—Clock skew modeling is important in the performance evaluation and prediction of clock distribution networks. This paper addresses the problem of statistical skew modeling for general clock distribution networks in the presence of process variations. The only available statistical skew model is not suitable for modeling the clock skews of general clock distribution networks in which clock paths are not identical. The old model is also too conservative for estimating the clock skew of a well-balanced clock network that has identical but strongly correlated clock paths (for instance, a well-balanced H -tree). In order to provide a more accurate and more general statistical skew model for general clock distributions, we propose a new approach to estimating the mean values and variances of both clock skews and the maximal clock delay of general clock distribution networks. Based on the new approach, a closed-form model is also obtained for well-balanced H -tree clock distribution networks. The paths delay correlation caused by the overlapped parts of path lengths is considered in the new approach, so the mean values and the variances of both clock skews and the maximal clock delay are accurately estimated for general clock distribution networks. This enables an accurate estimate of yields of both clock skew and maximal clock delay to be made for a general clock distribution network.

Index Terms—Clock distribution network, clock skew, maximal clock delay, process variations, statistical modeling, yield.

I. INTRODUCTION

THE evolution of VLSI chips toward larger die sizes and faster clock speeds makes clock distribution an increasingly important issue [1]. A striking example of what can be accomplished with aggressive clock design is the DEC alpha chip, designed to operate at more than 600 MHz [2]. The advanced Pentium III and AMD Athlon processors now work above 1 GHz. At such high speeds, clock skew becomes a very significant problem. Clock skew may arise mainly from unequal clock path lengths to various modules and process variations that cause clock path delay variations [3], [4]. To model the clock skew, either a worst-case or a statistical approach may be utilized. A worst-case approach can usually cause an unnecessarily long clock period. In a statistical approach, on the other hand, the clock parameters may be chosen so that the probability of timing failure is very small, but not zero. This usually results

in a shorter clock period. The available literature dealing with statistical clock skew modeling [5], [6] approaches the problem from the standpoint that all clock paths are assumed to be identical and independent, so an upper bound of expected clock skew is obtained. For general clock distribution networks (CDNs), the clock paths may not be identical and they usually depend on each other as they may overlap at some parts of their length, so the old statistical model is not applicable to modeling the clock skews of these clock networks in which clock paths are not identical. The skew model is also too conservative when it is used to estimate the clock skew of a well-balanced CDN in which clock paths are identical but strongly correlated (e.g., the well-balanced H -tree CDNs [7], [8] which are commonly used to reduce the clock skew). For different level H -trees, the expected clock skews estimated by using the old model are considerably larger than the actual expected skews as shown in this paper. In the case where the clock frequency is limited by the skew rather than by the minimum time between two successive events propagated through the H -tree [8], the old model will result in an unnecessarily long clock period.

The clock period of a CDN is in general determined by both the clock skew and the maximal clock delay of the network. The focus of this paper is to provide a recursive approach to estimating the expected values and the variances of both the clock skews and the maximal clock delay of general CDNs. The paths delay correlation caused by the overlapped parts of path lengths is taken into account in the new estimates, so the mean values and the variances of both clock skews and the maximal clock delay of general clock distribution networks are accurately estimated by using the new approach. This enables an accurate estimate of yields of both clock skew and the maximal clock delay and, thus, the yield of clock period to be made for a general CDN.

The rest of the paper is organized as follows: A general skew model for clock distribution networks is described in Section II. A novel approach is presented in Section III-A for evaluating recursively the mean values and the variances of clock skew and the maximal clock delay of general CDNs. In Section III-B, closed-form expressions are derived for the mean values and variances of both clock skew and the maximal clock delay of well-balanced H -tree CDNs. The yield modeling of clock skew and the maximal clock delay is discussed in Section IV. Section V compares the simulation results and theoretical results of clock skew and the maximal clock delay for three typical CDNs, and Section VI summarizes the contributions of this paper.

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II. CLOCK SKEW MODELING

Due to variations in process parameters, the actual circuit delay will deviate from the designed value [9]. For a given CDN, let $t(l_0, l_i)$ denote the signal propagation time on the unique path from the clock source l_0 to the sink l_i . The maximal clock delay ξ and the minimal clock delay η of the CDN can be defined as

$$\xi = \max_i \{t(l_0, l_i)\} \quad (1)$$

$$\eta = \min_i \{t(l_0, l_i)\}. \quad (2)$$

The clock skew between two sinks l_i and l_j is the delay difference $|t(l_0, l_i) - t(l_0, l_j)|$ and clock skew χ of the CDN is in general defined as the maximum value of $|t(l_0, l_i) - t(l_0, l_j)|$ over all sink pairs l_i and l_j in the CDN [10], [11]. Thus, χ is given by

$$\chi = \max_{i \neq j} |t(l_0, l_i) - t(l_0, l_j)| = \xi - \eta. \quad (3)$$

Process variations are subject to two sets of factors: systematic factors, like power supply fluctuations, which can be controlled by proper techniques and factors that are random, and therefore uncontrollable by improved techniques. Thus, the random factors determine the achievable performance of a circuit. Our major concern in this paper is to model the clock skew and maximal clock delay of general CDNs when the random factors are considered. When random process variations are considered, variations of paths delay are modeled by normal distributions [3], [12]. To model the clock skew χ , random variables ξ and η should be first characterized. The model developed in this paper is based on the following two assumptions.

- 1) A CDN can in general be represented by a binary tree, we assume that both the maximal clock delay and the minimal clock delay in each subtree (and also the whole binary tree) of the CDN can be modeled by normal distributions when process variations are considered. This assumption takes its roots in the available results [13], [14]. The assumption makes it easy to analyze the correlation that exists between the maximal and the minimal delay in a subtree. This correlation analysis is critical in determining the variance of skew in each subtree (and also the whole binary tree) of the CDN, and most importantly, the estimated results of clock skew and the maximal clock delay obtained by using the assumption are accurate as shown in this paper.
- 2) The delay along a clock path is the sum of the uncertain independent delays of the branches along the given path. Correlation between the delay of any two paths is determined only by the overlapped parts of their length.

The clock paths of a CDN usually have some common branches over their length, and these common branches cause correlation among the delays of these paths. The above assumption enables a complete analysis of this kind of correlation.

In addition to the delay correlation described in Assumption 2), the correlation among paths delay may also be caused by the correlated intra-die variations of these parameters involved

in that delay (e.g., threshold voltages, resistances, etc.). However, finding the correlation coefficient of these parameters is, in practice, quite cumbersome and may obscure the practicality of an approach considering all these kinds of correlation. We must be careful to avoid arriving at intractably complex models, so these kinds of correlation are neglected in this paper as indicated in Assumption 2). In general, the intra-die process parameters' correlation will lead to the paths delay in the same chip tending to be positive dependent. In this case, Assumption 2) will guarantee that the expected values of clock skew and maximal clock delay will still be upper bounded by the corresponding values estimated using our approach (see Appendix A for a discussion). Compared to the old upper bound of expected skew of a well-balanced CDN where all the clock paths are assumed completely independent, our estimates are enhanced significantly, as shown in this paper, because the paths delay correlation caused by the common branches of paths length are completely considered. Furthermore, the new approach is applicable to general CDNs, whereas the old model is only applicable to the well-balanced CDNs in which clock paths are identical.

From (3), the mean value and the variance of χ are given by [15]

$$E(\chi) = E(\xi) - E(\eta) \quad (4)$$

$$D(\chi) = D(\xi) + D(\eta) - 2 \cdot \rho \cdot \sqrt{D(\xi) \cdot D(\eta)}. \quad (5)$$

Here, $E(\cdot)$ and $D(\cdot)$ represent the mean value and the variance of a random variable, respectively, and ρ is the correlation coefficient of ξ and η . The parameters $E(\xi)$, $E(\eta)$, $D(\xi)$, $D(\eta)$, and ρ should be accurately estimated for a CDN to allow, in turn, the accurate modeling of clock skew and maximal clock delay.

III. A NEW APPROACH FOR PARAMETER ESTIMATION

A recursive approach for evaluating the parameters $E(\xi)$, $E(\eta)$, $D(\xi)$, $D(\eta)$ and ρ of general CDNs is presented here. Based on this algorithm, closed-form expressions of clock skews and the maximal clock delay of well-balanced H -tree CDNs are also developed.

A. Parameter Estimation Algorithm for General CDNs

A CDN can in general be represented by a binary tree, so a simplified binary tree shown in Fig. 1 is taken as an example to illustrate the evaluating process of these parameters. The evaluating process is then applied to general CDNs. All the paths in Fig. 1 are partitioned into independent branches s_0, s_1, s_2, \dots by the branch split points in the clock tree, where d_i is the actual delay of s_i . The branch split point (i, j) in the clock tree is associated with a set of random variables $(\xi_{ij}, \eta_{ij}, \chi_{ij})$, here ξ_{ij} , η_{ij} and χ_{ij} are the maximal clock delay, the minimal clock delay and the clock skew of the subtree starting from the split point, respectively. Each random variable here is characterized by both its mean value and its variance.

To illustrate that the parameters $E(\xi)$, $E(\eta)$, $D(\xi)$, $D(\eta)$ and ρ of the simplified binary clock tree can be evaluated recursively, we begin with the evaluating process of $(\xi_{00}, \eta_{00}, \chi_{00})$. Let branch s_i also be associated with a set of random variables, (ξ_i, η_i, ρ_i) with ξ_i being the maximal clock delay and η_i being

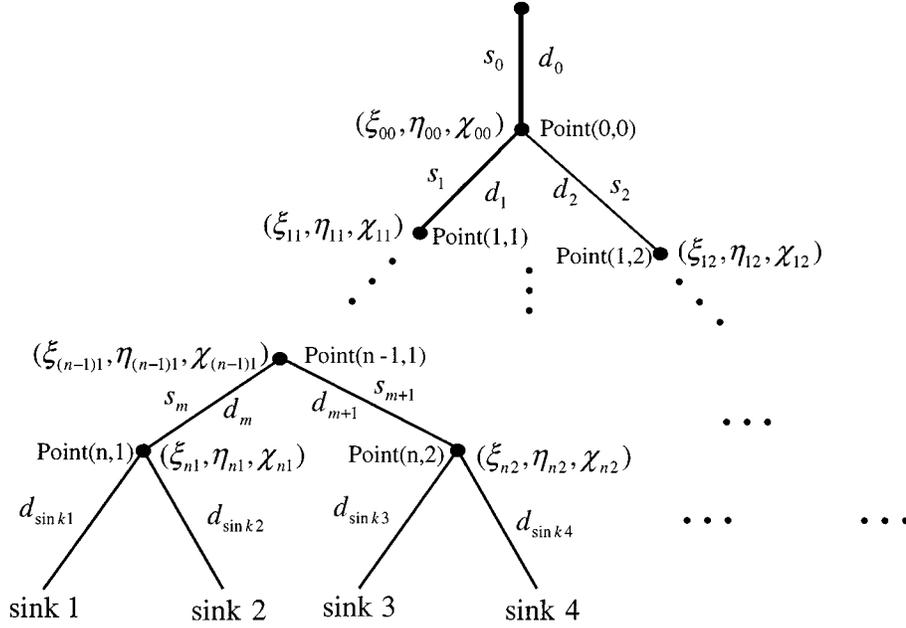


Fig. 1. Illustration of a simplified binary clock tree.

the minimal clock delay of the subtree starting from branch s_i , and ρ_i being the correlation coefficient of ξ_i and η_i . Thus

$$\begin{aligned} \xi_1 &= \xi_{11} + d_1, & \xi_2 &= \xi_{12} + d_2 \\ \eta_1 &= \eta_{11} + d_1, & \eta_2 &= \eta_{12} + d_2 \end{aligned} \quad (6)$$

$$\begin{aligned} \rho_1 &= \frac{D(\xi_1) + D(\eta_1) - D(\chi_{11})}{2\sqrt{D(\xi_1) \cdot D(\eta_1)}} \\ \rho_2 &= \frac{D(\xi_2) + D(\eta_2) - D(\chi_{12})}{2\sqrt{D(\xi_2) \cdot D(\eta_2)}}. \end{aligned} \quad (7)$$

Then we have

$$\xi_{00} = \max\{\xi_1, \xi_2\} = \frac{\xi_1 + \xi_2 + |\xi_1 - \xi_2|}{2}$$

$$\eta_{00} = \min\{\eta_1, \eta_2\} = \frac{\eta_1 + \eta_2 - |\eta_1 - \eta_2|}{2} \quad (8)$$

$$\chi_{00} = \xi_{00} - \eta_{00}. \quad (9)$$

Equations (6)–(9) indicate that the results $(\xi_{00}, \eta_{00}, \chi_{00})$ of branch split point (0, 0) are determined by and can be evaluated from both the corresponding results $[(\xi_{11}, \eta_{11}, \chi_{11})$ and $(\xi_{12}, \eta_{12}, \chi_{12})]$ of the next lower level split points (1, 1), (1, 2), and the delay of the branches $[s_1$ and $s_2]$ connecting the point to those next lower level split points (see Appendix B for the detailed evaluating process). So once the results of $(\xi_{ij}, \eta_{ij}, \chi_{ij})$ are obtained for each lowest-level split point (i.e., the split point from which no further branch split points can be found in the subtree starting from that split point), the process above can be used recursively to evaluate the mean values and the variances of clock skew, the maximal clock delay and the minimal clock delay of a general CDN in a bottom-up manner. In fact, the results of $(\xi_{n1}, \eta_{n1}, \chi_{n1})$ of one lowest-level split point $(n, 1)$ in Fig. 1 can be obtained as follows. The distribution functions of ξ_{n1} and η_{n1} can be obtained by using the same idea as for equa-

tions (B.1) and (B.2) in Appendix B, so the mean values and the variances of ξ_{n1} and η_{n1} can be evaluated by using their distribution functions, respectively. The mean value and the variance of χ_{n1} are given by (see Appendix C for the proof)

$$\begin{aligned} E(\chi_{n1}) &= E(\xi_{n1} - \eta_{n1}) = E(|d_{\text{sink}1} - d_{\text{sink}2}|) \\ &= \frac{2\sqrt{D_{\text{sink}k}}}{\sqrt{2\pi}} \exp\left(-\frac{1}{2} \left(\frac{E_{\text{sink}k}}{\sqrt{D_{\text{sink}k}}}\right)^2\right) \end{aligned} \quad (10)$$

$$+ \frac{2|E_{\text{sink}k}|}{\sqrt{2\pi}} \int_0^{|E_{\text{sink}k}|/\sqrt{D_{\text{sink}k}}} \exp\left(-\frac{1}{2}t^2\right) dt$$

$$\begin{aligned} D(\chi_{n1}) &= D(|d_{\text{sink}1} - d_{\text{sink}2}|) \\ &= E_{\text{sink}k}^2 + D_{\text{sink}k} - [E(\chi_{n1})]^2 \end{aligned} \quad (11)$$

where

$$\begin{aligned} E_{\text{sink}k} &= E(d_{\text{sink}1}) - E(d_{\text{sink}2}) \\ D_{\text{sink}k} &= D(d_{\text{sink}1}) + D(d_{\text{sink}2}). \end{aligned} \quad (12)$$

Based on the results of $(\xi_{00}, \eta_{00}, \chi_{00})$, the parameters $E(\xi)$, $E(\eta)$, $D(\xi)$, $D(\eta)$ and ρ of the whole binary tree are then given by

$$\begin{aligned} E(\xi) &= E(\xi_{00}) + E(d_0), & E(\eta) &= E(\eta_{00}) + E(d_0) \\ D(\xi) &= D(\xi_{00}) + D(d_0), & D(\eta) &= D(\eta_{00}) + D(d_0) \end{aligned} \quad (13)$$

$$\rho = \frac{D(\xi) + D(\eta) - D(\chi_{00})}{2\sqrt{D(\xi) \cdot D(\eta)}}. \quad (14)$$

The pseudocode for the parameter estimation algorithm can be summarized as follows:

Algorithm

Parameter estimation for general CDNs

Initialization: for each $Lp \in V$ do $\{\xi^b \leftarrow d^b, \eta^b \leftarrow d^b, \rho^b \leftarrow 1\}$ while $(V$ not empty) do

{ for each $Lp \in V$ do

$$p_{\xi^{Lp}}(x) = p(\xi_1^b < x) \cdot p(\xi_2^b < x)$$

$$p_{\eta^{Lp}}(x) = 1 - p(\eta_1^b > x) \cdot p(\eta_2^b > x)$$

$$E(\xi^{Lp}) = \int_{-\infty}^{+\infty} x \cdot d(p_{\xi^{Lp}}(x))$$

$$D(\xi^{Lp}) = \int_{-\infty}^{+\infty} [x - E(\xi^{Lp})]^2 \cdot d(p_{\xi^{Lp}}(x)),$$

$$E(\eta^{Lp}) = \int_{-\infty}^{+\infty} x \cdot d(p_{\eta^{Lp}}(x))$$

$$D(\eta^{Lp}) = \int_{-\infty}^{+\infty} [x - E(\eta^{Lp})]^2 \cdot d(p_{\eta^{Lp}}(x)),$$

$$\text{Cov}(\xi^{Lp}, \eta^{Lp}) = \text{Cov} \left(\frac{\xi_1^b + \xi_2^b + |\xi_1^b - \xi_2^b|}{2}, \frac{\eta_1^b + \eta_2^b + |\eta_1^b - \eta_2^b|}{2} \right)$$

$$E(\chi^{Lp}) = E(\xi^{Lp}) - E(\eta^{Lp}),$$

$$D(\chi^{Lp}) = D(\xi^{Lp}) + D(\eta^{Lp}) - 2 \cdot \text{Cov}(\xi^{Lp}, \eta^{Lp}).$$

Remove $G^{Lp} = (V^{Lp}, E^{Lp})$ from $G = (V, E)$

$$\xi^b \leftarrow \xi^{Lp} + d^{Lp}, \quad \eta^b \leftarrow \eta^{Lp} + d^{Lp}$$

$$E(\xi^b) \leftarrow E(\xi^{Lp}) + E(d^{Lp}), \quad E(\eta^b) \leftarrow E(\eta^{Lp}) + E(d^{Lp})$$

$$D(\xi^b) \leftarrow D(\xi^{Lp}) + D(d^{Lp}), \quad D(\eta^b) \leftarrow D(\eta^{Lp}) + D(d^{Lp})$$

$$\rho^b \leftarrow \frac{D(\xi^b) + D(\eta^b) - D(\chi^{Lp})}{2\sqrt{D(\xi^b) \cdot D(\eta^b)}}$$

}.

In the pseudocode, a CDN is represented by graph $G = (V, E)$ with vertex (split point) set V and edge (branch) set E . The lowest level split point Lp of the graph is associated with random variables $(\xi^{Lp}, \eta^{Lp}, \chi^{Lp})$ as defined above. (ξ^b, η^b, ρ^b) are the random variables associated with the branches starting from a lowest level splitting point, with $(\xi_1^b, \eta_1^b, \rho_1^b)$ and $(\xi_2^b, \eta_2^b, \rho_2^b)$ representing the random variables associated with the two branches starting from Lp , respectively. For a CDN, the initial values of ξ^b and η^b are just the actual delay d^b of the branches that support sinks. d^{Lp} is the actual delay of the branch connecting Lp to its parent splitting point, and $G^{Lp} = (V^{Lp}, E^{Lp})$ is the subgraph starting from Lp .

Since the algorithm carries out the same amount of computation for each split point, the following conclusion can be obtained.

Theorem 1: The parameter estimation algorithm given above computes a network $G = (V, E)$ in $O(|V|)$ time.

The theorem indicates that the parameter estimation algorithm is computationally effective in estimating the parameters $E(\xi)$, $E(\eta)$, $D(\xi)$, $D(\eta)$ and ρ of a general CDN.

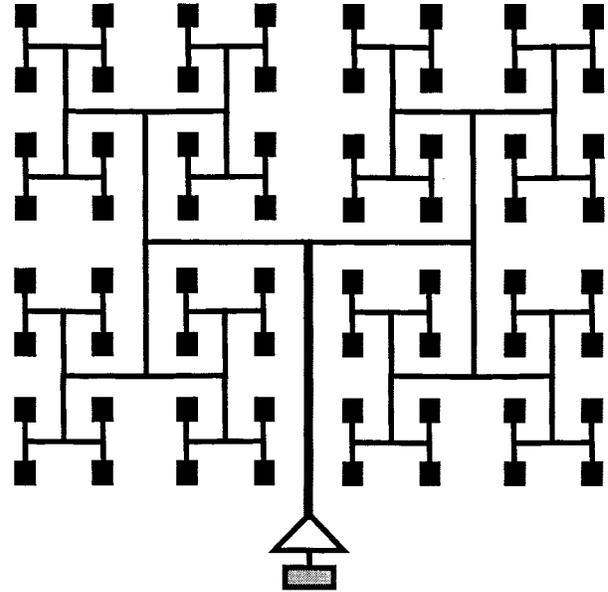


Fig. 2. An well-balanced H -tree clock distribution network for 64 processors (clock buffers are not illustrated here).

B. Parameter Estimation for H -Tree CDNs

The H -tree technique is widely used to reduce the clock skew [7], [8]. Due to the very symmetric structure of H -tree CDNs, it is possible for us to get a closed form model for both clock skew and the maximal clock delay of H -tree CDNs. Before developing the models, the H -tree itself must first be defined. Without loss of generality, a well-balanced H -tree has N hierarchical levels, where N denotes the tree depth. The level zero branch corresponds to the root branch, and level N branches to the branches that support sinks. A level i branch begins with a level i split point and ends with level $i+1$ split point. The H -tree illustrated in Fig. 2 is drawn for $N = 6$, which is used to distribute the clock signals to 64 processors.

For a N level well-balanced H -tree, let d_i , $i = 0, \dots, N$ be the actual delay of branch i of a clock path. The mean values and the variances of the maximal clock delay ξ and the minimal clock delay, η , of the H -tree are then given by following equations (see Appendix D for the derivation):

$$E(\xi) = \sum_{i=0}^N E(d_i) + \frac{1}{\sqrt{\pi}} \sum_{i=1}^N \sqrt{\sum_{k=1}^i \left(\frac{\pi-1}{\pi}\right)^{k-1} \cdot D(d_{N-i+k})} \quad (15)$$

$$E(\eta) = \sum_{i=0}^N E(d_i) - \frac{1}{\sqrt{\pi}} \sum_{i=1}^N \sqrt{\sum_{k=1}^i \left(\frac{\pi-1}{\pi}\right)^{k-1} \cdot D(d_{N-i+k})} \quad (16)$$

$$D(\xi) = D(\eta) = \sum_{i=0}^N \left(\frac{\pi-1}{\pi}\right)^i \cdot D(d_i). \quad (17)$$

Results (15)–(17) and (3) indicate that the expected clock skew $E(\chi)$ and skew variance $D(\chi)$ of the N level well-balanced

TABLE I
SOME MAJOR PROCESS PARAMETERS AND THEIR INTRADIE STANDARD DEVIATIONS (SD) OF A TYPICAL 0.25 μm CMOS PROCESS

Parameters	L_{eff} (μm)	V_{DD} (V)	V_{TN} (V)	V_{TP} (V)	t_{ox} (\AA)	μ_n ($\text{cm}^2/\text{V}\cdot\text{s}$)	μ_p ($\text{cm}^2/\text{V}\cdot\text{s}$)	t (f_{ox}) (μm)
Mean	0.25	2.5	0.51	-0.51	50	391	122	0.1
SD	0.0075	0	0.02	0.02	0.65	7.82	2.44	0.0013

H -tree are given by

$$E(\chi) = E(\xi) - E(\eta)$$

$$= \frac{2}{\sqrt{\pi}} \sum_{i=1}^N \sqrt{\sum_{k=1}^i \left(\frac{\pi-1}{\pi}\right)^{k-1} \cdot D(d_{N-i+k})} \quad (18)$$

$$D(\chi) = D(\xi) + D(\eta) - 2 \cdot \rho \cdot \sqrt{D(\xi) \cdot D(\eta)}$$

$$= 2 \cdot (1 - \rho) \cdot \sum_{i=0}^N \left(\frac{\pi-1}{\pi}\right)^i \cdot D(d_i) \quad (19)$$

where ρ is the correlation coefficient of ξ and η , and ρ can be recursively evaluated for a network as discussed in Section III-A. The closed-form expressions (15)–(19) indicate clearly how the clock skew and the maximal clock delay are accumulated along the clock paths and with the increase of H -tree size. This enables a suitable H -tree size to be selected for a specified clock frequency, and also enables minimization of the clock period, improving the speed for a fixed size H -tree network [16].

IV. MODELING THE YIELDS OF CLOCK SKEW AND THE MAXIMAL CLOCK DELAY

The clock period of a CDN is in general determined by both the clock skew and the maximal clock delay of the network. With the estimates of mean values and variances of both ξ and χ in hand, it is possible for us to estimate the yields of ξ and χ , and thus the yield of clock period. Here, the yield of a random variable means the probability that the variable is less than a specified value. As indicated in Assumption 1), the yield of ξ can be estimated by a normal distribution $N(E(\xi), D(\xi))$ with mean, $E(\xi)$, and variance, $D(\xi)$. For general CDNs, ξ and η are positively correlated (i.e., $\rho > 0$) normal variables [17], and clock skew χ can be modeled by log-normal distribution as verified by extensive simulation results [14]. The clock skew yield, i.e., the probability that the actual skew of the network, χ , is less than a skew specification x ($P(\chi < x)$), can then be evaluated as

$$P(\chi < x) = \int_0^x \frac{\log e}{\sqrt{2\pi} \cdot \delta_1 \cdot t} \exp \left[-\frac{1}{2} \left(\frac{\log t - \mu_1}{\delta_1} \right)^2 \right] dt. \quad (20)$$

Here, parameters μ_1 and δ_1 are given by [18]

$$\mu_1 = \log \left(\frac{[E(\chi)]^2}{\sqrt{D(\chi) + [E(\chi)]^2}} \right) \quad (21)$$

$$\delta_1 = \sqrt{\log e \cdot \log \left(\frac{D(\chi) + [E(\chi)]^2}{[E(\chi)]^2} \right)}. \quad (22)$$

Once the mean values and variances of both ξ and χ of a CDN are estimated by the algorithm developed in Section III, the yields of ξ and χ can be approximated by normal distribution and log-normal distribution, respectively.

The delay of the branch may then be obtained by averaging the rise and fall times. Here R_0 is the output resistance of the driving transistor of minimum size inverter, C_0 is the input capacitance of the driven minimum size inverter, C_{int} and R_{int} are the capacitance and resistance of the interconnection line in the branch. R_0 , C_0 , and R_{int} are given by

$$R_0 = \frac{1}{K \cdot (V_{DD} - V_T)}, \quad K = \frac{\mu \cdot C_{\text{ox}} \cdot W_T}{L_T}, \quad C_{\text{ox}} = \frac{\epsilon}{t_{\text{ox}}} \quad (24)$$

$$C_0 = C_{\text{ox}} \cdot W_T \cdot L_T, \quad R_{\text{int}} = r \cdot L / W \cdot t \quad (25)$$

where

W_T and L_T	width and length of the transistor;
C_{ox}	gate unit area capacitance;
t_{ox}	gate oxide thickness;
μ	charge carrier mobility;
V_T	threshold voltage;
r	metal resistivity;
ϵ	oxide dielectric constant.

Here, the interconnection line is with width W , length L , and thickness t on an oxide layer of thickness f_{ox} , and C_{int} can be estimated by the following empirical formula including the contribution of fringing fields [21]:

$$C_{\text{int}} = \epsilon \cdot L \cdot \left[\left(\frac{W}{f_{\text{ox}}} \right) + 0.77 + 1.06 \cdot \left(\frac{W}{f_{\text{ox}}} \right)^{0.25} + 1.06 \cdot \left(\frac{t}{f_{\text{ox}}} \right)^{0.5} \right]. \quad (26)$$

The process parameters and their standard deviations used here are based on the 0.25- μm CMOS technology predicted by the International Technology Roadmap for Semiconductors (ITRS) [22] and the MOSIS parametric test results of a typical 0.25 μm technology [23]. The mean values and intra-die standard deviations (SD) of these process parameters are presented in Table I.

Here, V_{DD} is not considered as a random variable since the power supply in a system is globally controlled. Furthermore, the standard deviation of the width of a transistor is 0.02 μm for n-MOS and 0.05 μm for p-MOS as estimated from MOSIS, and the standard deviation of L (length of interconnection line) is assumed to be 2% of its nominal. The n-MOS transistor and p-MOS transistor in the minimum inverter of the technology are assumed to have the gate width/length of 0.37 $\mu\text{m}/0.25 \mu\text{m}$ and 1.1 $\mu\text{m}/0.25 \mu\text{m}$, respectively.

As indicated in Assumption 2) the intra-die parameters correlations are neglected in this paper. Thus, R_0 (the output resistance of the driving transistor of minimum size inverter) in (23) will be independent from C_0 (the input capacitance of the driven minimum size inverter). One approach to calculating the delay variance of a branch due to the variations of process parameters is to first express the relation (23) in terms of independent variables (geometrical dimensions of the interconnection line in the branch, R_0 and C_0). The delay variance of the branch can then be determined in terms of variances of these independent random variables [3], [24]. For example, the variance, δ_z^2 , of a random variable Z that is a function of independent random variables, $z = f(x, y, \dots)$, may be obtained from

$$\delta_z^2 = \left(\frac{\partial f}{\partial x}\right)^2 \cdot \delta_x^2 + \left(\frac{\partial f}{\partial y}\right)^2 \cdot \delta_y^2 + \dots \quad (27)$$

Now consider the variances of C_0 and R_0 . Since $C_0 = C_{\text{ox}} \cdot W_T \cdot L_T$, all factors in this expression are independent variables. The variance of C_0 can be determined in terms of variances of these independent random variables using (27). By (24), R_0 is determined by parameters K , V_T , and V_{DD} . In a system, the power supply is controlled globally and is not a random variable. Since K and V_T are both dependent on C_{ox} , they are correlated variables. Also, for the gain constant, $K = \mu \cdot C_{\text{ox}} \cdot W_T / L_T$, of the transistor, the mobility μ has a t_{ox} dependence due to the impact of the vertical gate field and thus correlated to C_{ox} . Considering this correlation can lead to a more accurate estimation of variance of R_0 . For a simplified computation, however, we will neglect this correlation here because K and V_T , μ and C_{ox} can be roughly considered as independent variables as discussed in [3], [25]–[27]. Thus, the variance of K can be determined by the variances of μ , C_{ox} , W_T and L_T , and the variance of R_0 can then be evaluated from the variances of K and V_T using (27). Following similar arguments as above, we can also evaluate the mean delay value of a branch based on both (23) and the distributions of the basic parameters in (24)–(26) (geometrical parameters of both transistor and interconnection line, μ , t_{ox} , V_T , and f_{ox}). Here, each basic parameter is considered as a normal variable, but the process is also applied to other distributions.

Once the mean delay value and the delay variance of each branch are evaluated for a network, the theoretical approach developed in this paper can be used to estimate the mean values, the variances and the yields of both the clock skew and maximal clock delay of the network. In the theoretical approach, algorithms presented in Section III are first used to evaluate the parameters $E(\xi)$, $E(\eta)$, $D(\xi)$, $D(\eta)$, and ρ of different networks, then the yields of the clock skew and the maximal clock delay are estimated using the models provided in Section IV.

To verify the new approach, transistor level Monte Carlo simulations are also conducted. In the simulation, each basic parameter in (24)–(26) is simulated by a normal random variable. To agree with the conditions used in the theoretical approach, the correlation between K and V_T , and between μ and C_{ox} is neglected as discussed above. The actual delay of a branch is then evaluated from the random values of these basic param-

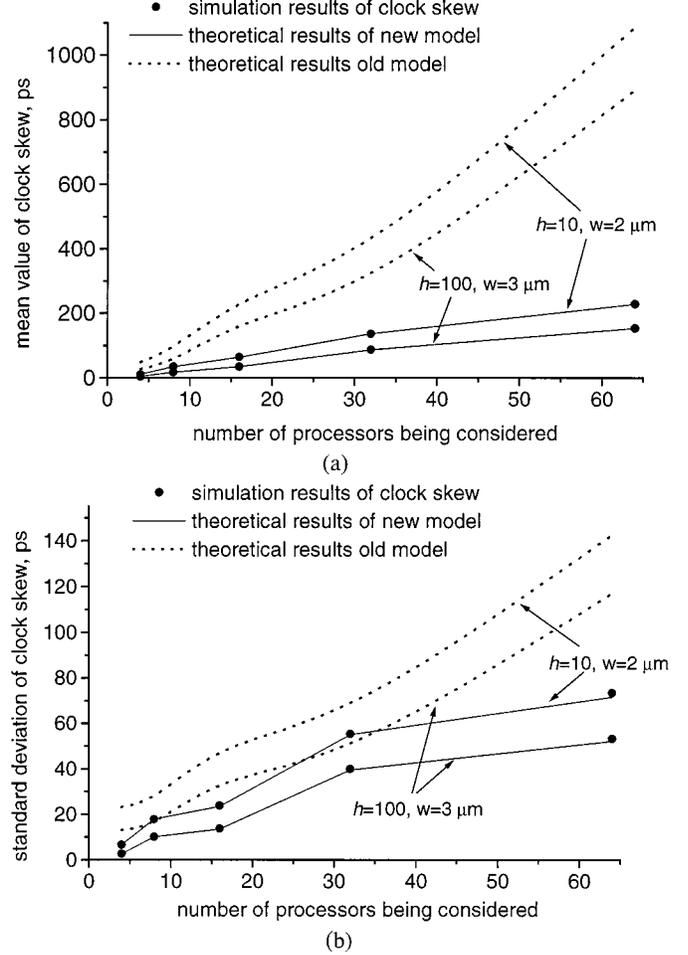


Fig. 3. Simulation results and theoretical results of clock skew of H -tree networks when different numbers of processors are considered. (a) Mean value of clock skew. (b) Standard deviation of clock skew.

eters using (23)–(26). The actual delay of a path is the sum of the actual delays of the branches along that path. The actual maximal clock delay, minimal clock delay and clock skew of the network are then determined by (1)–(3). For a specified value, the yield of a parameter (clock skew or the maximal clock delay) is estimated by the ratio of number of simulations in which the parameter is less than the specified value to the total number of simulations.

The first network considered is well known as the H -tree approach shown in Fig. 2 (for brevity, inverters are not illustrated in the following networks). Due to the very symmetrical design of H -tree clock networks, all clock paths within the H -tree are identical, and the old statistical model [5], [6] can be used to get an upper bound of its expected clock skew when all the paths are assumed to be independent. According to the old model, an upper bound of expected clock skew $E^{\text{upper}}(\chi)$ of a well-balanced H -tree is asymptotically given by [6]

$$E^{\text{upper}}(\chi) = \delta \cdot \left[\frac{4 \ln M - \ln \ln M - \ln 4\pi + 2C}{(2 \ln M)^{1/2}} + O\left(\frac{1}{\log M}\right) \right]. \quad (28)$$

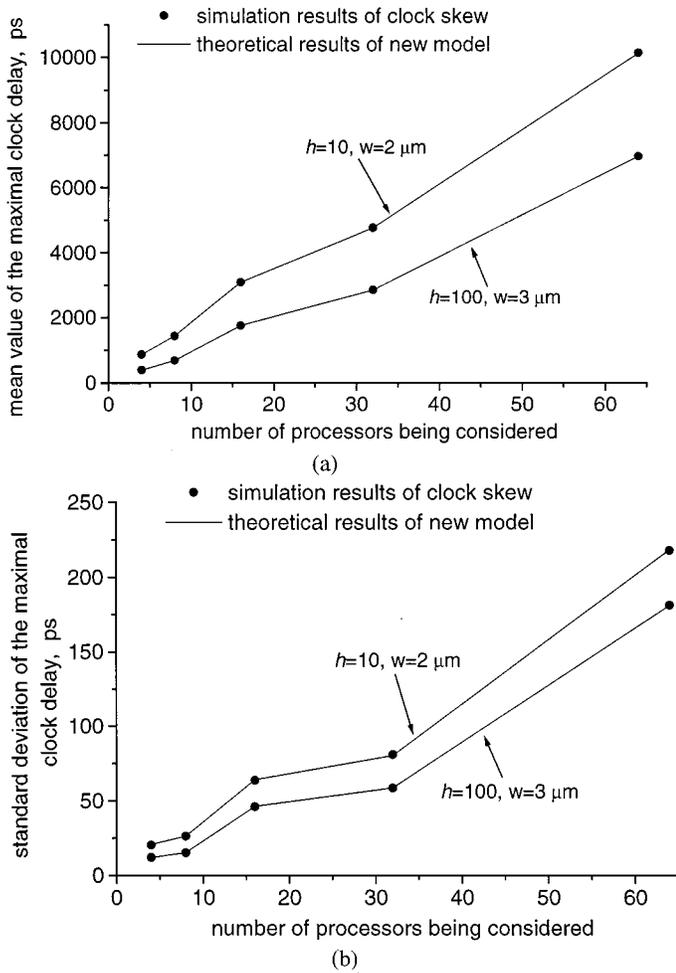


Fig. 4. Simulation results and theoretical results of the maximal clock delay of H -tree networks when different numbers of processors are considered. (a) Mean value of the maximal clock delay. (b) Standard deviation of the maximal clock delay.

With the variance of clock skew being given by

$$D^{\text{upper}}(\chi) = \frac{\pi^2 \delta^2}{6 \ln M} + O\left(\frac{1}{\log^2 M}\right) \quad (29)$$

where

- δ standard deviation of path delay;
- $C \approx 0.5772$ Euler's constant;
- M number of paths;
- $O(\cdot)$ higher order term.

In a N -level H -tree, there are a total of $2^{N+1} - 1$ branches, and it can be used to distribute clock signals to 2^N elements. For two combinations of parameters h and W , in a wide range, and when the numbers of processors are 4, 8, 16, 32, and 64, the theoretical results (obtained using both the old and new models) and simulation results of clock skews of corresponding H -trees are summarized in Fig. 3(a) and (b). The equivalent results for the maximal delay of the H -trees are summarized in Fig. 4(a) and (b).

The results in Figs. 3 and 4 show that the new model is accurate in estimating the mean values and standard deviations of both the clock skew and the maximal clock delay of H -tree CDNs, where the delay correlation determined by

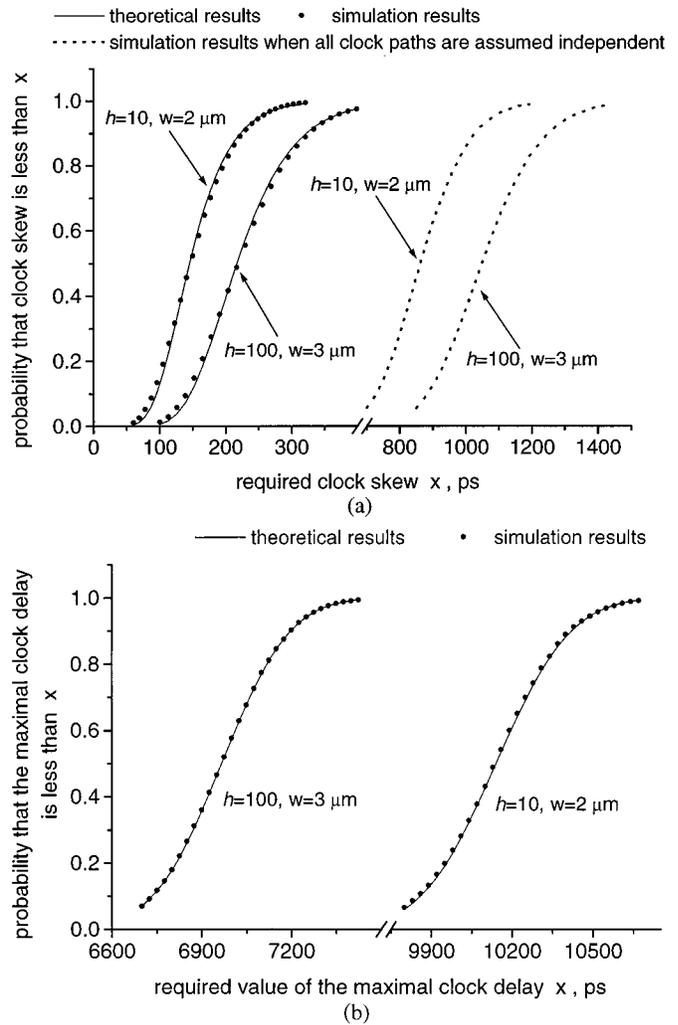


Fig. 5. Simulation yield results and theoretical yield results of clock skew and maximal clock delay of an H -tree network for two combinations of parameters h and W . (a) Yield results of clock skew. (b) Yield results of the maximal clock delay.

the overlapped parts of path lengths has been considered as indicated in Assumption 2). Compared to the old estimates of expected clock skew where all the paths in the H -tree are assumed completely independent, the new estimates based on Assumption 2) are a significant enhancement. For different sized H -trees, the expected clock skews estimated using the old model (28) are at least 2.6 times the expected clock skews estimated using our approach. This is shown in Fig. 3(a). In cases where clock frequency is limited by skew rather than by the minimum time between two successive events propagated through the H -tree [8], an unnecessarily long clock period will result from using the old skew model.

Based on the above estimated results of the mean values and the variances of both χ and ξ , the yields of χ and ξ can be further estimated as discussed in Section IV. For the six-level H -tree shown in Fig. 2, the theoretical yield results and the simulation yield results of both χ and ξ are summarized in Fig. 5(a) and (b). For comparison, we also present in Fig. 5(a) the simulation results of yield of clock skew when all paths are assumed independent.

The results in Fig. 5(a) indicate that the old model's independent assumption leads to very conservative estimates of clock

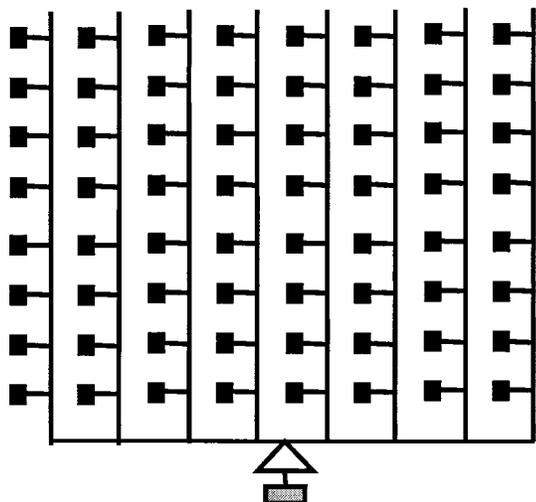


Fig. 6. Tree-type network.

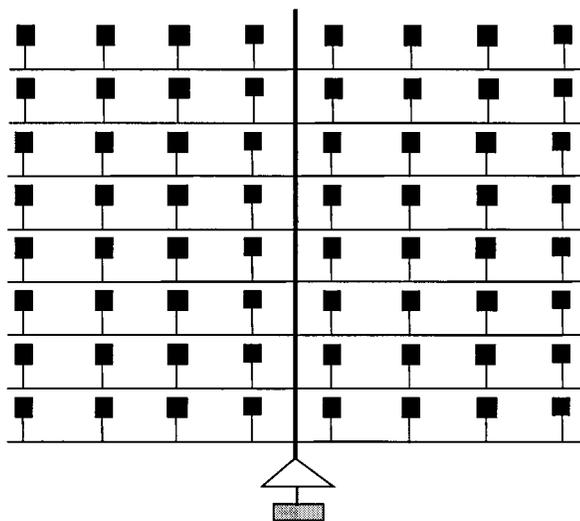


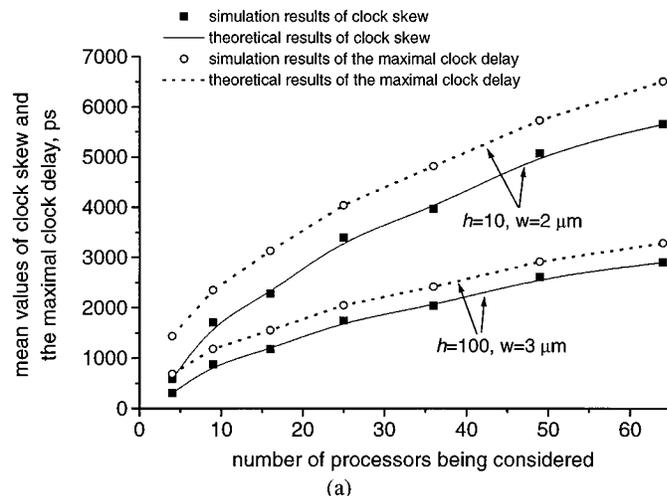
Fig. 7. Trunk-type network.

skew yields of H -tree CDNs that have identical but strongly correlated clock paths. The results in Fig. 5 also show that when the mean values and the variances of both the χ and ξ of H -tree CDNs are accurately estimated by our approach, the yields of their χ and ξ are further approximated by log-normal distribution and normal distributions, respectively.

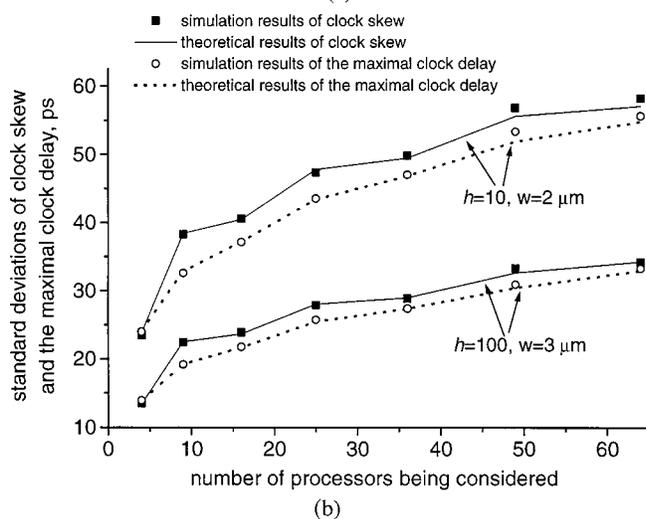
The next two network considered are the Tree-type network (Fig. 6) and Trunk-type network (Fig. 7). Since the paths in the two general CDNs are not identical, the old model (28) and (29) could not be used to model the skews of these networks. Thus, only the theoretical results of the new approach and the simulation results are illustrated for the following two CDNs.

In a Tree-type network, a single clock input drives a row of columns, and each of these columns drives same number of processors. When a Tree-type network is used to distribute clock signals to an $n \times n$ array of processors, a total of $2n^2 + 2^{\lfloor n/2 \rfloor}$ branches will be needed.

The Trunk-type network involves dividing the processors into two equal parts. A single clock drives a main trunk that is used to drive signals across each sub row placed at either sides of the trunk. In a Trunk-type network used for clock distribution for



(a)



(b)

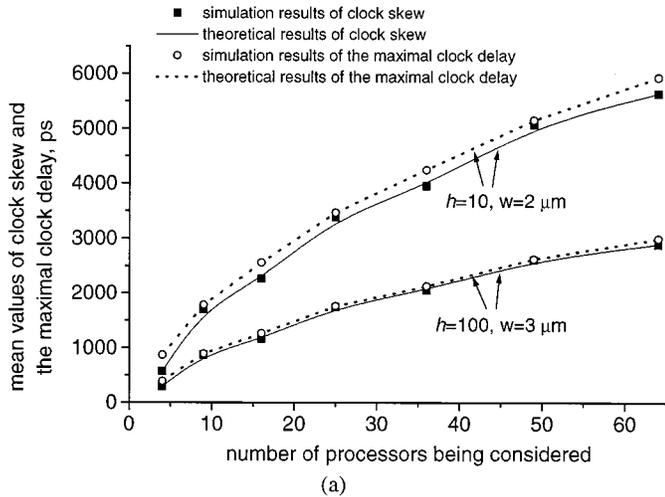
Fig. 8. Mean values and standard deviations of clock skew and maximal clock delay of Tree-type networks when different numbers of processors are considered. (a) Mean values of clock skew and maximal clock delay. (b) Standard deviations of clock skew and maximal clock delay.

an $n \times n$ array of processors, there are a total of $2n^2 + n - 1$ branches.

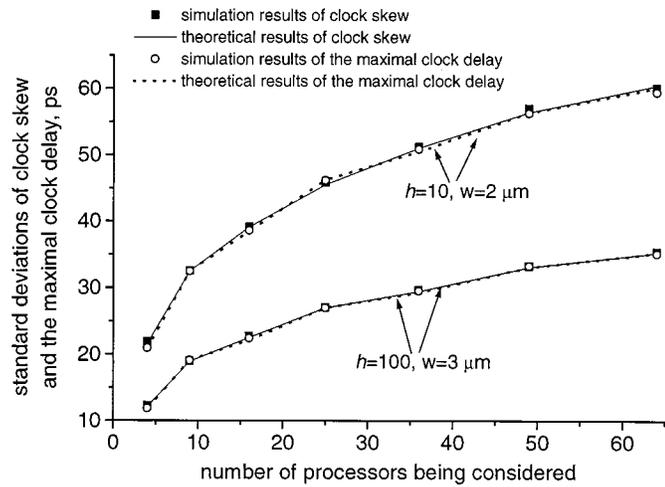
For the same combinations of parameters h and W used above for H -tree and when the array size varies from 2×2 to 8×8 , the theoretical results and the simulation results for clock skew and maximal clock delay of Tree-type networks are summarized in Fig. 8. The corresponding results of Trunk-type networks are summarized in Fig. 9.

The results in Figs. 8 and 9 indicate that the new model is also accurate in estimating the mean values and standard deviations of both χ and ξ for Tree-type CDNs and Trunk-type CDNs. For the Tree-type network shown in Fig. 6, the theoretical yield results and the simulation yield results of both χ and ξ are further summarized in Fig. 10. The corresponding results of the Trunk-type networks shown in Fig. 7 are summarized in Fig. 11.

Again, the results in Figs. 10 and 11 indicate that when the mean values and the variances of both χ and ξ are estimated accurately for Tree-type and Trunk-type networks, the yields of their χ and ξ are modeled by log-normal and normal distributions, respectively.



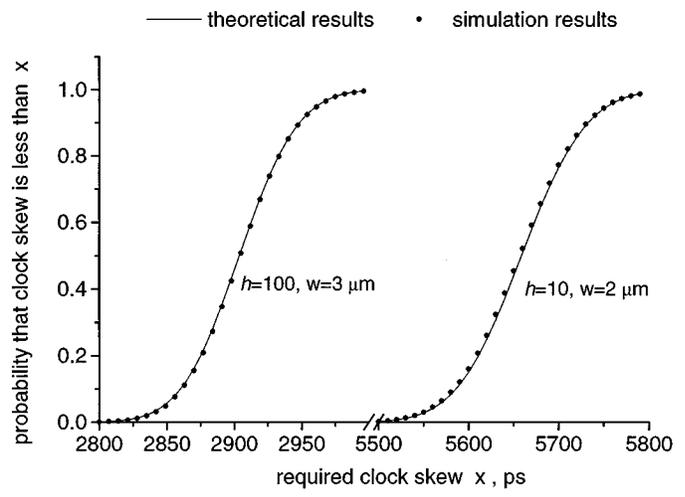
(a)



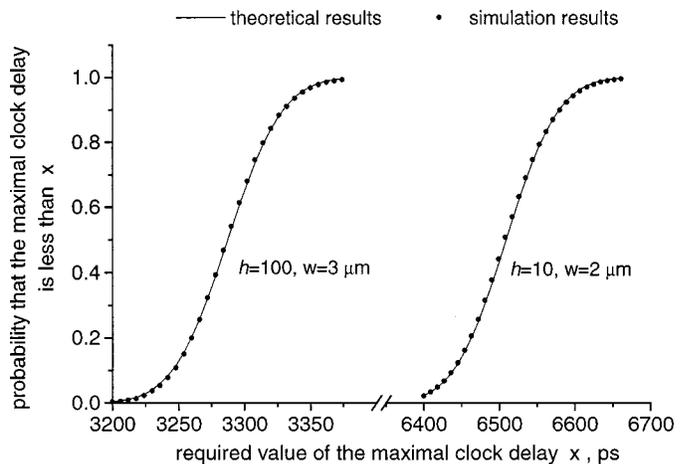
(b)

Fig. 9. Mean values and standard deviations of clock skew and maximal clock delay of Trunk-type networks when different number of processors is considered. (a) Mean values of clock skew and maximal clock delay. (b) Standard deviations of clock skew and maximal clock delay.

Due to the assumption that all clock paths are identical, the old statistical skew model could not be used to model the clock skews of general clock networks with nonidentical paths. The new model developed in this paper, however, can be used to accurately estimate the mean values and the variances of both clock skew and the maximal clock delay of these general CDNs. For a well-balanced CDN (e.g., H -tree clock network), the expected clock skews estimated by old model are very conservative because correlation among paths delay are completely neglected. On the other hand, the expected clock skews estimated by the new model are enhanced significantly. For the well-balanced H -tree network shown in Fig. 2, the results in Figs. 3(a) and 4(a) show that when parameters $h = 100$ and $W = 3 \mu\text{m}$, the actual mean value of maximal clock delay is 6.96 ns, and the actual mean value of clock skew is 153.4 ps. The expected clock skew estimated by old model is about 892.5 ps, a value 5.8 times larger than the actual value. For a traditional clocking mode and when the 10% rule of thumb relating the skew to the clock period is used, the actual clock period should be dominated by the maximal clock delay, and the mean value of clock period will be 6.96 ns. However, when the old skew model is used in the



(a)



(b)

Fig. 10. Simulation yield results and theoretical yield results of clock skew and maximal clock delay of a Tree-type network for two combinations of parameters h and W . (a) Yield results of clock skew. (b) Yield results of maximal clock delay.

skew estimate, the clock period should be determined by the clock skew rather than the maximal clock delay, and the mean value of clock period will be 8.925 ns. The old model will thus mislead efforts to reduce the clock period of the network. For a pipelined clocking mode, the clock periods of well-balanced H -tree networks will be dominated by the clock skew rather than by the minimum time between two successive events propagated through the H -tree, an unnecessarily long clock period will result from using the old skew model.

V. CONCLUSION

The available statistical skew model is too conservative in estimating the expected skew of a well-balanced CDN, the model is also not general enough to model the clock skew of a non-balanced CDN. A computationally effective approach is presented for estimating the mean values and the variances of both clock skew and the maximal clock delay of general CDNs. Closed form models of clock skew and maximal clock delay are also presented for well-balanced H -tree CDNs. The paths delay correlation determined by the overlapped parts of path lengths is completely

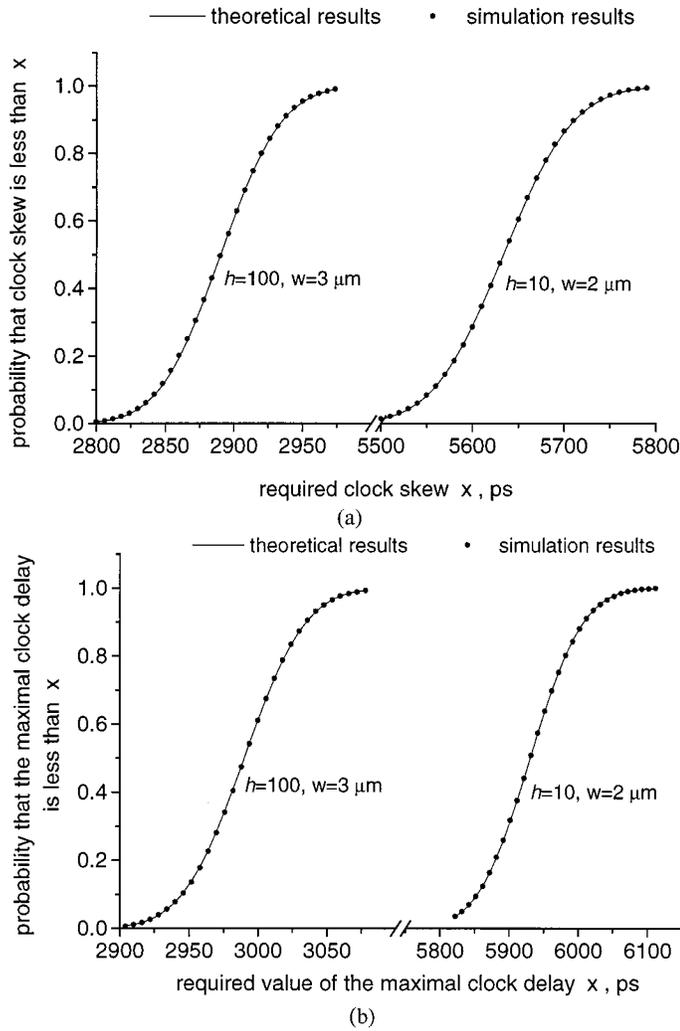


Fig. 11. Simulation yield results and theoretical yield results of clock skew and maximal clock delay of a Trunk-type network for two combinations of parameters h and W . (a) Yield results of clock skew. (b) Yield results of maximal clock delay.

considered in the new approach so the mean values and variances of both clock skew and maximal clock delay are accurately estimated for general CDNs. It is further verified that when the mean values and variances of both clock skew and maximal clock delay of a CDN are accurately estimated by the new approach, the skew yield and maximal delay yield of the CDN are approximated by log-normal and normal distributions, respectively. This enables the clock period yield of the CDN to be estimated. If process variations are considered in designing a clock distribution network, mean values and variances of delays for all branches should carefully estimated, then the approach presented here will be useful in evaluating and predicting the network's performance of clock skew and the maximal clock delay.

APPENDIX A

First, we need the following lemma [5].

Lemma 1: Let $F_A(x)$ and $F_B(x)$ be the probability distribution functions for random variables A and B respectively, and suppose further that $F_A(x)$ and $F_B(x)$ are differentiable and A and B have finite means and variances. If $F_A(x) \geq F_B(x)$

for all x , then $E(A) \leq E(B)$. [Here $E(\cdot)$ and $D(\cdot)$ represent the mean value and the variance of a random variable, respectively.]

The correlated intra-die parameters variations mean that the increase of a parameter's values in one area tend to be associated with the increase of the parameter's values in other areas of a chip, and vice versa. This will lead to the positive dependence between delays d_A and d_B of two paths A and B in the chip, then we have

$$\begin{aligned} P(d_A < x | d_B < x) &\geq P(d_A < x) \\ P(d_A > x | d_B > x) &\geq P(d_A > x) \end{aligned} \quad (\text{A.1})$$

where $P(\cdot)$ is the probability that an event happens.

A CDN can be represented by a binary tree, so a simplified binary tree shown in Fig. 1 is taken as example for illustration. All the paths in Fig. 1 are partitioned into branches s_0, s_1, s_2, \dots by the branch split points in the clock tree, where d_i is the actual delay of s_i . The branch split point (i, j) in the clock tree is associated with a set of random variables $(\xi_{ij}, \eta_{ij}, \chi_{ij})$, here ξ_{ij} , η_{ij} and χ_{ij} are the maximal clock delay, the minimal clock delay and the clock skew of the subtree starting from the split point, respectively. We begin with the subtree which starts from the lowest level split point $(n, 1)$. When the intra-die parameters correlation is considered, the delays $d_{\text{sin}k1}$ and $d_{\text{sin}k2}$ will be positive dependent so we have

$$\begin{aligned} P(\xi_{n1} < x) &= P(d_{\text{sin}k1} < x, d_{\text{sin}k2} < x) \\ &= P(d_{\text{sin}k1} < x) \cdot P(d_{\text{sin}k2} < x | d_{\text{sin}k1} < x) \\ &\geq P(d_{\text{sin}k1} < x) \cdot P(d_{\text{sin}k2} < x) \end{aligned} \quad (\text{A.2})$$

$$\begin{aligned} P(\eta_{n1} < x) &= 1 - P(\eta_{n1} \geq x) \\ &= 1 - P(d_{\text{sin}k1} \geq x, d_{\text{sin}k2} \geq x) \\ &= 1 - P(d_{\text{sin}k1} \geq x) \cdot P(d_{\text{sin}k2} \geq x | d_{\text{sin}k1} \geq x) \\ &\leq 1 - P(d_{\text{sin}k1} \geq x) \cdot P(d_{\text{sin}k2} \geq x). \end{aligned} \quad (\text{A.3})$$

If Assumption 2) is used, $d_{\text{sin}k1}$ and $d_{\text{sin}k2}$ are independent, and the distribution functions of ξ_{n1} and η_{n1} will be $P(d_{\text{sin}k1} < x) \cdot P(d_{\text{sin}k2} < x)$ and $1 - P(d_{\text{sin}k1} \geq x) \cdot P(d_{\text{sin}k2} \geq x)$, respectively. By Lemma 1 and (A.2), (A.3), the expected value of the maximal clock delay ($E(\xi_{n1})$) and the expected value of the clock skew ($E(\chi_{n1}) = E(\xi_{n1} - \eta_{n1}) = E(\xi_{n1}) - E(\eta_{n1})$) of the subtree will be upper bounded by the corresponding values estimated using Assumption 2). Since we always have $E(d_m + \xi_{n1}) = E(d_m) + E(\xi_{n1})$ and $E((d_m + \xi_{n1}) - (d_m + \eta_{n1})) = E(\chi_{n1})$ whether d_m is dependent or independent with $d_{\text{sin}k1}$ and $d_{\text{sin}k2}$, the expected values of the maximal clock delay and clock skew of the subtree starting from branch s_m will also be upper-bounded by the corresponding values estimated using Assumption 2), and the same conclusion will apply to the subtree starting from branch s_{m+1} .

Furthermore, if the intra-die parameters correlation is considered, the delay of a path in the subtree starting from branch s_m will be positive dependent with the delay of a path in the subtree starting from branch s_{m+1} . Following similar arguments as for that of the subtree starting from the lowest level split point $(n, 1)$, the expected values of clock skew and the maximal clock

delay of the subtree starting from point $(n - 1, 1)$ will also be upper bounded by the corresponding values estimated by Assumption 2).

By applying the arguments above to the binary-tree recursively, we conclude that, if the intra-die parameters correlation are considered, the expected values of clock skew and the maximal clock delay of each subtree (and also the whole binary tree) of the CDN tree will be upper-bounded by the corresponding values estimated using Assumption 2).

APPENDIX B

Part 1—Evaluation of $E(\xi_{00})$, $D(\xi_{00})$, $E(\eta_{00})$, $D(\eta_{00})$ and $E(\chi_{00})$: Since

$$\xi_i = \xi_{1i} + d_i, \quad \eta_i = \eta_{1i} + d_i, \quad i = 1, 2.$$

The following results can be obtained by using the Assumption 2):

$$E(\xi_i) = E(\xi_{1i}) + E(d_i), \quad E(\eta_i) = E(\eta_{1i}) + E(d_i)$$

$$D(\xi_i) = D(\xi_{1i}) + D(d_i), \quad D(\eta_i) = D(\eta_{1i}) + D(d_i)$$

$$i = 1, 2$$

$$\rho_1 = \frac{D(\xi_1) + D(\eta_1) - D(\chi_{11})}{2\sqrt{D(\xi_1) \cdot D(\eta_1)}}$$

$$\rho_2 = \frac{D(\xi_2) + D(\eta_2) - D(\chi_{12})}{2\sqrt{D(\xi_2) \cdot D(\eta_2)}}.$$

Since

$$\xi_{00} = \max\{\xi_1, \xi_2\}, \quad \eta_{00} = \min\{\eta_1, \eta_2\}.$$

The distribution function $F_{\xi_{00}}(x)$ of ξ_{00} and distribution function $F_{\eta_{00}}(x)$ of η_{00} are given by

$$F_{\xi_{00}}(x) = P(\xi_{00} < x) = P(\xi_1 < x) \cdot P(\xi_2 < x)$$

$$= \frac{1}{2\pi\sqrt{D(\xi_1) \cdot D(\xi_2)}} \cdot \left(\int_{-\infty}^x \exp \left[-\frac{1}{2} \left(\frac{t - E(\xi_1)}{\sqrt{D(\xi_1)}} \right)^2 \right] dt \right) \cdot \left(\int_{-\infty}^x \exp \left[-\frac{1}{2} \left(\frac{t - E(\xi_2)}{\sqrt{D(\xi_2)}} \right)^2 \right] dt \right) \quad (\text{B.1})$$

$$F_{\eta_{00}}(x) = P(\eta_{00} < x) = 1 - P(\eta_1 > x) \cdot P(\eta_2 > x)$$

$$= 1 - \frac{1}{2\pi\sqrt{D(\eta_1) \cdot D(\eta_2)}} \cdot \left(\int_x^{+\infty} \exp \left[-\frac{1}{2} \left(\frac{t - E(\eta_1)}{\sqrt{D(\eta_1)}} \right)^2 \right] dt \right) \cdot \left(\int_x^{+\infty} \exp \left[-\frac{1}{2} \left(\frac{t - E(\eta_2)}{\sqrt{D(\eta_2)}} \right)^2 \right] dt \right). \quad (\text{B.2})$$

Thus, the parameters $E(\xi_{00})$, $D(\xi_{00})$, $E(\eta_{00})$, and $D(\eta_{00})$ can be obtained by using their distribution functions, respectively. Based on the results above, the mean value of χ_{00} is determined by

$$E(\chi_{00}) = E(\xi_{00} - \eta_{00}) = E(\xi_{00}) - E(\eta_{00}).$$

Part 2—Evaluation of $D(\chi_{00})$: The variance of χ_{00} is given by

$$D(\chi_{00}) = D(\xi_{00} - \eta_{00}) = D(\xi_{00}) + D(\eta_{00}) - 2\text{Cov}(\xi_{00}, \eta_{00})$$

Here $\text{Cov}(\xi_{00}, \eta_{00})$ is the covariance of ξ_{00} and η_{00} , and the evaluation of $\text{Cov}(\xi_{00}, \eta_{00})$ is the main computational problem of $D(\chi_{00})$. To evaluate the covariance, ξ_{00} and η_{00} are first expressed as

$$\xi_{00} = \frac{\xi_1 + \xi_2 + |\xi_1 - \xi_2|}{2}, \quad \eta_{00} = \frac{\eta_1 + \eta_2 - |\eta_1 - \eta_2|}{2}.$$

Then $\text{Cov}(\xi_{00}, \eta_{00})$ is evaluated from (B.3) as shown at the bottom of the page, where ρ_1 is the correlation coefficient of ξ_1 and η_1 , ρ_2 is the correlation coefficient of ξ_2 and η_2 . The $\text{Cov}(|\xi_1 - \xi_2|, |\eta_1 - \eta_2|)$ in (B.3) can be evaluated as follows. Since normal random variables ξ_1 and η_1 are independent from normal random variables ξ_2 and η_2 , $\xi_1 - \xi_2$ is modeled by normal $N(E_\xi, D_\xi)$ with mean, E_ξ , and variance, D_ξ , and $\eta_1 - \eta_2$ is modeled by normal $N(E_\eta, D_\eta)$.

Here

$$E_\xi = E(\xi_1) - E(\xi_2), \quad D_\xi = D(\xi_1) + D(\xi_2)$$

$$E_\eta = E(\eta_1) - E(\eta_2), \quad D_\eta = D(\eta_1) + D(\eta_2).$$

The covariance $\text{Cov}(\xi_1 - \xi_2, \eta_1 - \eta_2)$ of $\xi_1 - \xi_2$ and $\eta_1 - \eta_2$ is given by

$$\text{Cov}(\xi_1 - \xi_2, \eta_1 - \eta_2) = \rho_1 \sqrt{D(\xi_1)D(\eta_1)} + \rho_2 \sqrt{D(\xi_2)D(\eta_2)}.$$

$$\text{Cov}(\xi_{00}, \eta_{00}) = \text{Cov} \left(\frac{\xi_1 + \xi_2 + |\xi_1 - \xi_2|}{2}, \frac{\eta_1 + \eta_2 - |\eta_1 - \eta_2|}{2} \right)$$

$$= \frac{1}{4} \left[\rho_1 \cdot \sqrt{D(\xi_1)D(\eta_1)} - \text{Cov}(\xi_1, |\eta_1 - \eta_2|) + \rho_2 \sqrt{D(\xi_2)D(\eta_2)} - \text{Cov}(\xi_2, |\eta_1 - \eta_2|) \right] + \text{Cov}(|\xi_1 - \xi_2|, \eta_1) + \text{Cov}(|\xi_1 - \xi_2|, \eta_2) - \text{Cov}(|\xi_1 - \xi_2|, |\eta_1 - \eta_2|) \quad (\text{B.3})$$

Then the correlation coefficient λ_1 of $\xi_1 - \xi_2$ and $\eta_1 - \eta_2$ is given by

$$\lambda_1 = \frac{\sqrt{D(\xi_1)D(\eta_1)} \cdot \rho_1 + \sqrt{D(\xi_2)D(\eta_2)} \cdot \rho_2}{\sqrt{D_\xi \cdot D_\eta}}.$$

Thus, the relation between $\xi_1 - \xi_2$ and $\eta_1 - \eta_2$ is given by [15]

$$\frac{\xi_1 - \xi_2 - E_\xi}{\sqrt{D_\xi}} = \lambda_1 \cdot \frac{\eta_1 - \eta_2 - E_\eta}{\sqrt{D_\eta}} + \sqrt{1 - \lambda_1^2} \cdot Z$$

where Z is a standard normal variable independent from $\eta_1 - \eta_2$. Then we have

$$|\xi_1 - \xi_2| = |b_1(\eta_1 - \eta_2) + \sqrt{D_1} \cdot Z|. \quad (\text{B.4})$$

Here, the function $b_1(x)$ and parameter D_1 are defined as

$$b_1(x) = \lambda_1 \cdot \frac{\sqrt{D_\xi}}{\sqrt{D_\eta}} \cdot (x - E_\eta) + E_\xi$$

$$D_1 = (1 - \lambda_1^2) \cdot D_\xi.$$

The covariance $\text{Cov}(|\xi_1 - \xi_2|, |\eta_1 - \eta_2|)$ is defined as

$$\begin{aligned} \text{Cov}(|\xi_1 - \xi_2|, |\eta_1 - \eta_2|) &= \int_0^{+\infty} \int_0^{+\infty} [x - E(|\eta_1 - \eta_2|)] \cdot [y - E(|\xi_1 - \xi_2|)] \\ &\quad \cdot d[F_1(x, y)] \end{aligned}$$

where $F_1(x, y)$ is the joint distribution function of $|\xi_1 - \xi_2|$ and $|\eta_1 - \eta_2|$. From (B.4), $F_1(x, y)$ is given by

$$\begin{aligned} F_1(x, y) &= P(|\eta_1 - \eta_2| < x, |\xi_1 - \xi_2| < y) \\ &= P(|\eta_1 - \eta_2| < x) \cdot P(|\xi_1 - \xi_2| < y | |\eta_1 - \eta_2| < x) \\ &= \int_{-x}^x \left[\int_{(-y-b_1(t))/\sqrt{D_1}}^{(y-b_1(t))/\sqrt{D_1}} \frac{1}{\sqrt{2\pi}} \exp\left(-\frac{t_1^2}{2}\right) \cdot dt_1 \right] \\ &\quad \cdot \frac{1}{\sqrt{2\pi \cdot D_\eta}} \exp\left(-\frac{(t - E_\eta)^2}{2D_\eta}\right) dt. \end{aligned}$$

The joint density function $f_1(x, y)$ of $|\xi_1 - \xi_2|$ and $|\eta_1 - \eta_2|$ is determined as

$$\begin{aligned} f_1(x, y) &= \frac{1}{2\pi \sqrt{D_\eta \cdot D_1}} \cdot \exp\left[-\frac{1}{2} \left(\frac{x - E_\eta}{\sqrt{D_\eta}}\right)^2\right] \\ &\quad \cdot \left\{ \exp\left[-\frac{1}{2} \left(\frac{y - b_1(x)}{\sqrt{D_1}}\right)^2\right] \right. \\ &\quad \left. + \exp\left[-\frac{1}{2} \left(\frac{y + b_1(x)}{\sqrt{D_1}}\right)^2\right] \right\} \\ &\quad + \frac{1}{2\pi \sqrt{D_\eta \cdot D_1}} \cdot \exp\left[-\frac{1}{2} \left(\frac{x + E_\eta}{\sqrt{D_\eta}}\right)^2\right] \end{aligned}$$

$$\begin{aligned} &\cdot \left\{ \exp\left[-\frac{1}{2} \left(\frac{y - b_1(-x)}{\sqrt{D_1}}\right)^2\right] \right. \\ &\quad \left. + \exp\left[-\frac{1}{2} \left(\frac{y + b_1(-x)}{\sqrt{D_1}}\right)^2\right] \right\}. \end{aligned}$$

So the covariance $\text{Cov}(|\xi_1 - \xi_2|, |\eta_1 - \eta_2|)$ can be evaluated from

$$\begin{aligned} \text{Cov}(|\xi_1 - \xi_2|, |\eta_1 - \eta_2|) &= \int_0^{+\infty} \int_0^{+\infty} [x - E(|\eta_1 - \eta_2|)] \cdot [y - E(|\xi_1 - \xi_2|)] \\ &\quad \cdot f_1(x, y) dx dy. \end{aligned}$$

Here, $E(|\xi_1 - \xi_2|)$ and $E(|\eta_1 - \eta_2|)$ are given by the following (see Appendix C for the proof):

$$\begin{aligned} E(|\xi_1 - \xi_2|) &= \frac{2\sqrt{D_\xi}}{\sqrt{2\pi}} \exp\left(-\frac{1}{2} \left(\frac{E_\xi}{\sqrt{D_\xi}}\right)^2\right) \\ &\quad + \frac{2|E_\xi|}{\sqrt{2\pi}} \int_0^{|E_\xi|/\sqrt{D_\xi}} \exp\left(-\frac{1}{2} t^2\right) dt \\ E(|\eta_1 - \eta_2|) &= \frac{2\sqrt{D_\eta}}{\sqrt{2\pi}} \exp\left(-\frac{1}{2} \left(\frac{E_\eta}{\sqrt{D_\eta}}\right)^2\right) \\ &\quad + \frac{2|E_\eta|}{\sqrt{2\pi}} \int_0^{|E_\eta|/\sqrt{D_\eta}} \exp\left(-\frac{1}{2} t^2\right) dt. \end{aligned}$$

It can be proven in the same way as that for $\text{Cov}(|\xi_1 - \xi_2|, |\eta_1 - \eta_2|)$, that the covariance $\text{Cov}(\xi_1, |\eta_1 - \eta_2|)$ is given by

$$\begin{aligned} \text{Cov}(\xi_1, |\eta_1 - \eta_2|) &= \int_{-\infty}^{+\infty} \int_0^{+\infty} [x - E(\xi_1)] \cdot [y - E(|\eta_1 - \eta_2|)] \\ &\quad \cdot f_2(x, y) dx dy \end{aligned} \quad (\text{B.5})$$

where

$$\begin{aligned} f_2(x, y) &= \frac{1}{2\pi \sqrt{D(\xi_1) \cdot D_2}} \\ &\quad \cdot \left\{ \exp\left[-\frac{1}{2} \left(\frac{y - b_2(x)}{\sqrt{D_2}}\right)^2\right] \right. \\ &\quad \left. + \exp\left[-\frac{1}{2} \left(\frac{y + b_2(x)}{\sqrt{D_2}}\right)^2\right] \right\} \\ &\quad \cdot \exp\left[-\frac{1}{2} \left(\frac{x - E(\xi_1)}{\sqrt{D(\xi_1)}}\right)^2\right] \end{aligned} \quad (\text{B.6})$$

$$\begin{aligned} b_2(x) &= \lambda_2 \cdot \sqrt{\frac{D(\eta_1) + D(\eta_2)}{D(\xi_1)}} \cdot [x - E(\xi_1)] \\ &\quad + E(\eta_1) - E(\eta_2) \end{aligned} \quad (\text{B.7})$$

$$\lambda_2 = \rho_1 \cdot \sqrt{\frac{D(\eta_1)}{D(\eta_1) + D(\eta_2)}},$$

$$D_2 = (1 - \lambda_2^2) \cdot [D(\eta_1) + D(\eta_2)]. \quad (\text{B.8})$$

$\text{Cov}(\xi_2, |\eta_1 - \eta_2|)$, $\text{Cov}(\eta_1, |\xi_1 - \xi_2|)$ and $\text{Cov}(\eta_2, |\xi_1 - \xi_2|)$ can be evaluated as for $\text{Cov}(\xi_1, |\eta_1 - \eta_2|)$. To evaluate $\text{Cov}(\xi_2, |\eta_1 - \eta_2|)$, ξ_1 and ρ_1 in (B.5)–(B.8) should be replaced by ξ_2 and ρ_2 , respectively. To evaluate $\text{Cov}(\eta_1, |\xi_1 - \xi_2|)$, ξ_1 , η_1 and η_2 in (B.5)–(B.8) should be replaced by η_1 , ξ_1 and ξ_2 , respectively. Finally, to evaluate $\text{Cov}(\eta_2, |\xi_1 - \xi_2|)$, ξ_1 , η_1 , η_2 and ρ_1 in (B.5)–(B.8) should be replaced by η_2 , ξ_1 , ξ_2 and ρ_2 , respectively.

APPENDIX C

Let R_1 and R_2 be two independent normal random variables, and let $R = R_1 - R_2$. Then R is also a normal random variable with its mean, μ , and its standard deviation, δ , given by

$$\mu = E(R) = E(R_1) - E(R_2),$$

$$\delta = \sqrt{D(R)} = \sqrt{D(R_1) + D(R_2)}.$$

The distribution function $F_{|R|}(x)$ of $|R|$ can be determined as

$$F_{|R|}(x) = P(|R| < x) = \frac{1}{\sqrt{2\pi} \cdot \delta} \int_{-x}^x \exp\left[-\frac{1}{2} \left(\frac{t-\mu}{\delta}\right)^2\right] dt$$

$$x > 0.$$

So the density function $f_{|R|}(x)$ of $|R|$ is:

$$f_{|R|}(x) = \frac{1}{\sqrt{2\pi} \cdot \delta} \left\{ \exp\left[-\frac{1}{2} \left(\frac{x-\mu}{\delta}\right)^2\right] + \exp\left[-\frac{1}{2} \left(\frac{x+\mu}{\delta}\right)^2\right] \right\},$$

$$x > 0.$$

Thus, the mean value $E(|R|)$ of $|R|$ is given by

$$E(|R|) = \int_0^{+\infty} x \cdot f_{|R|}(x) dx$$

$$= \frac{2\delta}{\sqrt{2\pi}} \exp\left[-\frac{1}{2} \left(\frac{\mu}{\delta}\right)^2\right]$$

$$+ \frac{2|\mu|}{\sqrt{2\pi}} \int_0^{|\mu|/\delta} \exp\left(-\frac{1}{2} t^2\right) dt.$$

Then the variance $D(|R|)$ of $|R|$ can be evaluated as

$$D(|R|) = \int_0^{+\infty} [x - E(|R|)]^2 \cdot f_{|R|}(x) dx$$

$$= \int_0^{+\infty} x^2 \cdot f_{|R|}(x) dx - [E(|R|)]^2$$

$$= \mu^2 + \delta^2 - [E(|R|)]^2.$$

APPENDIX D

For the N hierarchical-level, well-balanced H -tree, let ξ_i be the maximal clock delay and η_i be the minimal clock delay of the sub H -tree starting from level i split point. Then we have

$$\xi_i = \max\{(d_{(i+1)1} + \xi_{(i+1)1}), (d_{(i+1)2} + \xi_{(i+1)2})\}$$

$$= \{(d_{(i+1)1} + \xi_{(i+1)1}) + (d_{(i+1)2} + \xi_{(i+1)2})$$

$$+ |(d_{(i+1)1} + \xi_{(i+1)1}) - (d_{(i+1)2} + \xi_{(i+1)2})|\}/2$$

$$\eta_i = \min\{(d_{(i+1)1} + \eta_{(i+1)1}), (d_{(i+1)2} + \eta_{(i+1)2})\}$$

$$= \{(d_{(i+1)1} + \eta_{(i+1)1}) + (d_{(i+1)2} + \eta_{(i+1)2})$$

$$- |(d_{(i+1)1} + \eta_{(i+1)1}) - (d_{(i+1)2} + \eta_{(i+1)2})|\}/2$$

where $d_{(i+1)1}$ and $d_{(i+1)2}$ are independent samples of $d_{(i+1)}$, $\xi_{(i+1)1}$ and $\xi_{(i+1)2}$ are independent samples of $\xi_{(i+1)}$, $\eta_{(i+1)1}$ and $\eta_{(i+1)2}$ are independent samples of $\eta_{(i+1)}$. Based on the property that two normal random variables are independent if and only if their covariance is zero [15], the following results can be obtained by using both the symmetry of well-balanced H -tree and Assumption 1)

$$E(\xi_i) = E(d_{i+1}) + E(\xi_{i+1}) + \frac{\sqrt{D(d_{i+1}) + D(\xi_{i+1})}}{\sqrt{\pi}} \quad (\text{D.1})$$

$$E(\eta_i) = E(d_{i+1}) + E(\eta_{i+1}) - \frac{\sqrt{D(d_{i+1}) + D(\eta_{i+1})}}{\sqrt{\pi}} \quad (\text{D.2})$$

$$D(\xi_i) = \frac{\pi - 1}{\pi} \cdot [D(d_{i+1}) + D(\xi_{i+1})],$$

$$D(\eta_i) = \frac{\pi - 1}{\pi} \cdot [D(d_{i+1}) + D(\eta_{i+1})]. \quad (\text{D.3})$$

The process above indicates clearly that $E(\xi_i)$, $D(\xi_i)$, $E(\eta_i)$ and $D(\eta_i)$ can be obtained using $E(\xi_{i+1})$, $D(\xi_{i+1})$, $E(\eta_{i+1})$, $D(\eta_{i+1})$, $E(d_{i+1})$, and $D(d_{i+1})$. By applying (D.1)–(D.3) to the N -level, well-balanced H -tree recursively, the mean values and the variances of the maximal clock delay, ξ , and the minimal clock delay η of the H -tree are then given by

$$E(\xi) = \sum_{i=0}^N E(d_i) + \frac{1}{\sqrt{\pi}} \sum_{i=1}^N$$

$$\cdot \sqrt{\sum_{k=1}^i \left(\frac{\pi - 1}{\pi}\right)^{k-1} \cdot D(d_{N-i+k})}$$

$$E(\eta) = \sum_{i=0}^N E(d_i) - \frac{1}{\sqrt{\pi}} \sum_{i=1}^N$$

$$\cdot \sqrt{\sum_{k=1}^i \left(\frac{\pi - 1}{\pi}\right)^{k-1} \cdot D(d_{N-i+k})}$$

$$D(\xi) = D(\eta) = \sum_{i=0}^N \left(\frac{\pi - 1}{\pi}\right)^i \cdot D(d_i).$$

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REFERENCES

- [1] E. G. Friedman, *Clock Distribution Networks in VLSI Circuits and Systems*. New York: IEEE, 1995.
- [2] D. W. Bailey and B. J. Benschneider, "Clocking design and analysis for a 600-MHz alpha microprocessor," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1627–1633, Dec. 1998.
- [3] M. Afghahi and C. Svensson, "Performance of synchronous and asynchronous schemes for VLSI systems," *IEEE Trans. Comput.*, vol. 41, pp. 858–872, July 1992.
- [4] M. Shoji, "Elimination of process-dependent clock skew in CMOS VLSI," *IEEE J. Solid-State Circuits*, vol. SC-21, pp. 875–880, Oct. 1986.
- [5] S. D. Kugelmass and K. Steiglitz, "A probabilistic model for clock skew," in *Proc. Int. Conf. Systolic Arrays*, San Diego, CA, May 1988, pp. 545–554.
- [6] —, "An upper bound of expected clock skew in synchronous system," *IEEE Trans. Comput.*, vol. 39, pp. 1475–1477, Dec. 1990.
- [7] A. L. Fisher and H. T. Kung, "Synchronizing large VLSI processor arrays," *IEEE Trans. Comput.*, vol. C-34, pp. 734–740, Aug. 1985.
- [8] M. Nekili, G. Bois, and Y. Savaria, "Pipelined H-trees for high-speed clocking of large integrated systems in presence of process variations," *IEEE Trans. VLSI Syst.*, vol. 5, pp. 161–174, June 1997.
- [9] M. D'Abreu, *et al.*, "Understanding of the fabrication process—Key to design and test of mixed signal ICs," in *Proc. Eur. Test Workshop*, Barcelona, Spain, May 1998.
- [10] A. B. Kahng and G. Robins, *On Optimal Interconnections for VLSI*. Norwell, MA: Kluwer, 1996.
- [11] A. Balboni, C. Costi, M. Pellencin, A. Quadrini, and D. Sciuto, "Clock skew reduction in ASIC logic design: A methodology for clock tree management," *IEEE Trans. Comput.-Aided Design Integrated Circuits Syst.*, vol. 17, pp. 344–356, Apr. 1998.
- [12] M. Eisele, J. Berthold, D. Schmitt-landsiedeld, and R. Mahnkopf, "The impact of intra-die device parameter variations on path delay and on the design for yield of low voltage digital circuits," *IEEE Trans. VLSI Syst.*, vol. 5, pp. 360–368, 1997.
- [13] T. Gneiting and I. P. Jalowiecki, "Influence of process parameter variations on the signal distribution behavior of wafer scale integration devices," *IEEE Trans. Components, Packaging, Manufacturing Technol.—Part B*, vol. 18, pp. 424–430, Aug. 1995.
- [14] X. H. Jiang and S. Horiguchi, "Distribution analysis of clock skew and clock delay for general clock distribution networks," JAIST Res. Rep. (ISSN.0918-7553) IS-RR-2000-014, June 2000.
- [15] J. Pitman, *Probability*. New York, 1993.
- [16] X. H. Jiang and S. Horiguchi, "Optimization of wafer scale H-tree clock distribution network based on a new statistical skew model," in *Proc. IEEE Int. Symp. Defect and Fault Tolerant in VLSI Systems (DFT'2000)*, Yamana, Japan, Oct. 2000, pp. 96–104.
- [17] —, "A recursive approach to estimating clock skew yield and clock delay yield for general clock distribution networks," JAIST Res. Rep. (ISSN.0918-7553) IS-RR-2000-010, Apr. 2000.
- [18] *Probability and Statistics*. New York: Academic, 1985.
- [19] N. Nigam and D. C. Keezer, "A comparative study of clock distribution approaches for VLSI," in *Proc. IEEE Int. Conf. Wafer Scale Integration*, San Francisco, CA, Jan. 1993, pp. 243–251.
- [20] H. Bbakoglu and J. D. Meindl, "Optimal interconnection circuits for VLSI," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 903–909, 1985.
- [21] N. H. E. Weste and K. Eshraghian, *Principles of CMOS VLSI Design: A Systems Perspective*. Reading, MA: Addison-Wesley, Apr. 1994.
- [22] International technology roadmap for semiconductors (ITRS) (1998). [Online]. Available: <http://public.itrs.net>
- [23] MOSIS (2000). [Online]. Available: <http://www.mosis.org>
- [24] A. Papoulis, *Probability, Random Variables and Stochastic Process*. New York: McGraw-Hill, 1965.
- [25] K. R. Lakshmi Kumar, A. Hadaway, and M. A. Copeland, "Characterization and modeling of mismatch in MOS transistors for precision analog design," *IEEE J. Solid-State Circuits*, vol. SC-21, pp. 1057–1066, Dec. 1986.
- [26] K. R. Lakshmi Kumar, "Characterization and modeling of mismatch in MOS devices and application to precision analog design," Ph.D. dissertation, Carlton Univ., Ottawa, ON, Canada, 1985.
- [27] J. Bastos, M. Steyaert, A. Pergoot, and W. Sansen, "Mismatch characterization of submicron MOS transistors," *Analog Integrated Circuits Signal Processing*, vol. 12, pp. 95–106, 1997.



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