

PAPER

Redundant Vias Insertion for Performance Enhancement in 3D ICs

Xu ZHANG^{†*}, Xiaohong JIANG^{†*}, *Nonmembers*, and Susumu HORIGUCHI^{†*}, *Member*

SUMMARY Three dimensional (3D) integrated circuits (ICs) have the potential to significantly enhance VLSI chip performance, functionality and device packing density. Interconnects delay and signal integrity issues are critical in chip design. In this paper, we extend the idea of redundant via insertion/placement in 3D ICs to minimize the propagation delay of interconnects with the consideration of signal integrity. The simulation results based on a 65nm CMOS technology demonstrate that our approach in general can result in a 9% improvement in average delay and a 26% decrease in reflection coefficient.

key words: 3D IC, redundant vias, via placement, delay, signal integrity, impedance matching

1. Introduction

Semiconductor chips have been facing constant pressure to improve their performance with a reduced power and cost. As technology node of VLSI scales, chip area and wire length continue to increase, causing increased interconnect delays. To overcome this problem, some methods such as repeater/buffer insertion and wire sizing have been developed. However, these methods will result in other problems like augmented power consumption and thermal integrity. All of the above problems can have deleterious implications on chip performance, reliability and design effort. Furthermore, such phenomena will be sustained or aggravated as clock frequencies of VLSI systems increase.

Three dimensional (3D) integrated circuits (ICs), which comprise multiple tiers of active devices, have the potential to enhance VLSI chip performance, functionality and device packing density [1]. For example, 3D ICs offer an attractive alternative to conventional 2D planar ICs: they can combine different technologies such as analog and digital circuits within the single chip cube to construct a multi-tier (multi-plane) system. Thus, using 3D ICs allows for integrating the best technology for a particular portion of an application into one chip package.

One of several promising solutions to 3D ICs is vertical integration, in which multiple layers of active devices are stacked with vertical interconnects between

tiers (planes) to form 3D integrated circuits. Depending on the fabrication technology, 3D ICs can be accomplished by different processes or schematics. For example, chip-level and wafer-level schematics based on face-to-face or face-to-back stacking have been proposed, where the stacked tiers are bonded with metal pads or blanket dielectric fusion bonding (or an adhesive interlayer) [1] to achieve interconnection between the neighboring tiers (wafers or chips). Fig.1 shows a schematic diagram of 3D IC structure implemented with a face-to-back process.

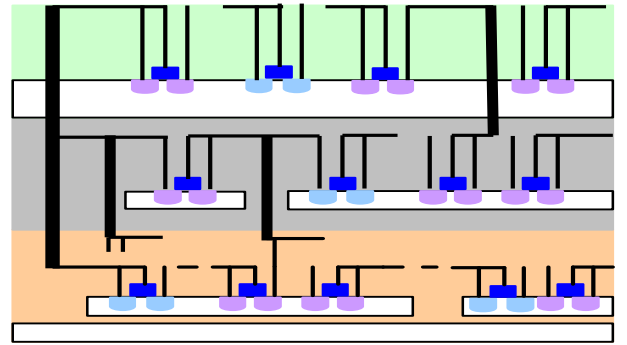


Fig. 1 The structure schematic of a 3-tiers' 3D IC fabricated with a face-to-back process (The thick vertical lines stand for through-hole vias for inter-tiers interconnections)

By expanding vertically rather than spreading in 2D planar area, obviously the delay of signal propagation in interconnects can be decreased due to the decreased length of interconnects in 3D ICs. Thus, the drawback of long interconnects in conventional 2D ICs can be alleviated. Additionally, 3D ICs technology can also result in a reduction of total active power, noise improvement and a greater logical span.

In 3D ICs, signal paths like wires for global clock distribution consist of multiple-segment interconnects routed in different tiers and some vertical inter-tier interconnects implemented by vertical through-hole vias (abbreviated as vias hereafter). Since each tier in 3D ICs may be fabricated with different technologies or processes, the impedance characteristics of different segments of the global interconnects may be disparate [1]. Furthermore, the impedance characteristics of vias may also be different from that of horizontal wires.

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[†]The authors are with the Graduate School of Information Science, Tohoku University, Sendai, 980-8579 Japan

*E-mail: {zhxu, jiang, susumu}@ecei.tohoku.ac.jp

Hence, the impedance characteristic of wires for inter-tier and global interconnects is actually not uniform [2] in 3D ICs.

Interconnects delay is crucial to the performance of modern digital VLSI systems, since it is a big fraction of total delay and it is in general increasing with technology scaling. To maximize performance improvement in 3D ICs, some approaches related to vias placement and wire routing have been proposed in presence of non-uniform impedance characteristics of interconnects. The authors in [3] assumed that the vertical wire (via) is in the middle of the net (wire) regardless of the length and impedance of the wire, and estimated the delay distribution in their 3D integration schematic with a RC delay model. Based on a geometric programming tool, Pavlidis *et al* [2] proposed an approach for vias placement to minimize the total delay of inter-tier interconnects with the consideration of the non-uniform impedance characteristics of interconnects. Their results showed an average performance improvement of 16% can be achieved, compared to the approach where vias are equally spaced in a wire. However, the important signal integrity issues due to the non-uniform impedance characteristics were not addressed in both [3] and [2]. It is notable that signal integrity issues such as reflection resulted by impedance discontinuities can be very deleterious to digital VLSI systems, since it may significantly affect the logical operation and reliability of a VLSI system.

Recently, Lee *et al* [4] proposed a novel approach for redundant via insertion to improve yield/reliability and manufacturability in traditional 2D ICs under via density constraints. This approach is an extension of conventional via insertion/placement, since it can help to decrease partial or complete via failure due to various reasons (like manufacturing process). According to their approach, the yield/reliability may be significantly improved by inserting redundant via properly without violating via density constraints.

In this paper, we extend the redundant via insertion in [4] to 3D ICs and propose an approach of redundant via placement/insertion to minimize the total delay for inter-tier or global interconnects. The issue of signal integrity due to the non-uniform impedance characteristics of interconnects is also carefully addressed. The main contributions of our work include:

- We extend the idea for redundant via insertion to 3D ICs, and propose an approach to minimizing the total interconnect delay based on the redundant via insertion/placement.
- We address signal integrity issues of interconnects with the consideration of non-uniform impedance characteristics in 3D ICs. In particular, we consider the signal reflection issues that may result in deleterious effects such as ring and undershoot, and propose impedance matching to decrease the

reflection coefficient based on the redundant via insertion.

- We formulate the above considerations to a multi-objective optimization and propose an efficient algorithm to solve it. In addition, we prove that the optimization related to our approach is practical.

The rest of this paper is organized as follows. Some preliminaries about 3D ICs and vias placement/insertion are introduced in Section 2. The problem formulation is described in Section 3. In Section 4, the simulation methodology is presented. The simulation results and discussion are provided in Section 5. Finally, in Section 6, we conclude this paper.

2. 3D ICs and Vias Placement/Insertion

Compared to the conventional planar ICs, 3D ICs are more suitable for the integration of heterogeneous materials, devices, signals and technologies. Usually, multiple tiers (also called planes) are included in a 3D IC, and these physical tiers are closely and vertically stacked using bonding process. In 3D ICs, interconnects routed in different tiers are connected with bonding medium (adhesive medium or metal pads) [1] to construct whole signal paths and achieve inter-tier communication. Therefore, the impedance characteristics of interconnects and vias may be very different from each other, namely, the impedance characteristics of inter-tier signal paths are non-uniform. Some approaches have been proposed in [3] and [2] to evaluate the impact of vias placement/insertion upon total delay in the presence of non-uniform impedance.

In the traditional 2D ICs, via discontinuities have a negligible effect on the propagated edge rate and the near end or far end coupled noise, and its effect on delay is also insignificant [5]. In 3D ICs, however, the height of a via can be as high as $20\mu m$ above [2], which is much longer than the vias in 2D ICs. Thus, the impedance characteristics of wires and vias in 3D ICs are very different, which may result in signal integrity issues such as signal reflection due to discontinuing impedance characteristics. For example, signal reflection occurs once the impedance characteristic alters in signal propagation path [6]. Therefore, it is necessary to consider the impacts of via on delay and signal integrity in 3D ICs to evaluate real performance of 3D integration VLSI systems.

Lee *et al* [4] proposed a redundant via insertion approach in 2D ICs using the methods of end-line extension and redundant vias insertion adjacent to a single via (we call these methods as redundant via insertion for simplicity hereafter). Fig.2 shows the structure of redundant via insertion when the line end extension is applied. In an 2D IC layout, a via provides the connection between net segments from neighboring metal layers. Partial or complete vias failure may occur due

to different reasons, such as cut misalignment and line-end shortening during a fabrication process, electromigration and thermal stress. As a consequence, these via failures usually result in an increased contact resistance and parasitic capacitance, or leave an open net in a circuit and invalidate the functionality of overall design. By redundant via insertion, both partial and complete vias failure can be alleviated. Exploiting the methods and algorithms proposed in [4], via density constraint will not be violated, while the yield/reliability and manufacturability can significantly be improved.

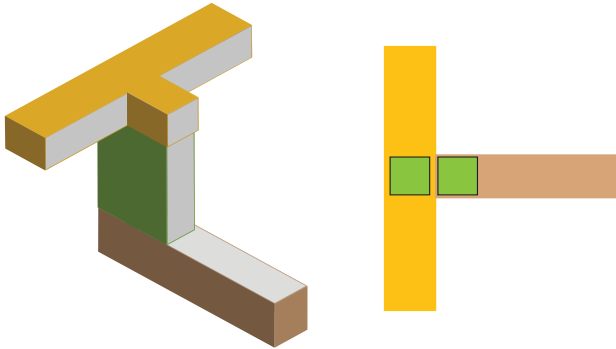


Fig. 2 Redundant via insertion (line end extension)

In vertical integration-based 3D ICs, the reliable formation of high-aspect-ratio (AR) vias are required to connect different wafers or chips to achieve communication among them [1]. However, all metallization techniques have their specific limitations on the maximum available aspect ratio of vias, which will result in an additional design constraint with respect to the layout of 3D ICs. Considering such a condition, it is necessary to pay attention to the issues of reliability and limitation of vias fabrication in 3D ICs, compared to vias in conventional planar VLSI systems. By the application of redundant vias insertion in 3D ICs, it is possible to decrease the aspect ratio of vias. Also, it can relax design constraint and improve the reliability and manufacturability/yield of 3D VLSI systems like that in 2D VLSI systems.

Moreover, by inserting a redundant via near the original via, the current handing capacity of via can be increased, and the impedance characteristic and parasitics of via may also be altered. Therefore, the idea about redundant via insertion introduced in [4] offers us an opportunity to conduct via sizing or vias insertion to minimize the delay and consider signal integrity simultaneously without violating via density constraint. For example, we can extend via size along the wire routing direction or the direction perpendicular to the wire routing direction in available routing area. It is similar to inserting an additional via at the side of original via (see Fig.3). Consequently, in this paper, we extend this idea to 3D ICs, and propose a redundant via insertion-based approach to minimizing the delay of inter-tier

interconnect while addressing also the signal integrity issues.

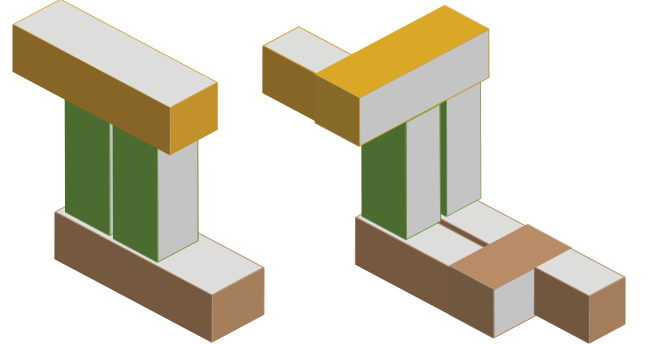


Fig. 3 Via sizing by redundant via insertion

3. Problem Formulation and Optimization

In this section, we first describe the delay calculation of inter-tier interconnects, then we introduce the impedance matching that is helpful for improving signal integrity. We summarize the problem formulation and propose the optimization method in Section 3.3.

3.1 Delay Modeling

Since the delay of interconnects is crucial to the performance of VLSI systems, it is important to find an optimum scheme of via placement for an interconnect in 3D ICs to minimize the total delay of the interconnect with the consideration of non-uniform impedance.

As the interconnect length and operating speed entered the nanoscale regime and gigascale regime, respectively, the inductance component becomes comparable to resistance component in circuits of VLSI (specially for Cu-based interconnect technology with a low resistance) [7]. Thus, the more advanced RLC model should be adopted to fully analyze the timing feature of interconnects.

In this paper, our primary goal is to minimize total signal propagation delay for given inter-tier interconnects. Without loss of generality, we consider a global inter-tier distributed RLC interconnect going through n tiers, as illustrated in Fig.4. Since buffer/repeater insertion is an efficient method to satisfy delay constraint for long wire, we assume that one inverter is inserted in each tier (please refer to Fig.4).

We use l_i ($i = 1, \dots, n$) to denote the length of segment that is routed in Tier i , and use h_i ($i = 1, \dots, n-1$) to denote the height of via that connects Tier i and Tier $(i+1)$. The sum of length of all the segments and the height of vias should be the total given length L , i.e.,

$$\sum_{i=1}^n l_i + \sum_{i=1}^{n-1} h_i = L \quad (1)$$

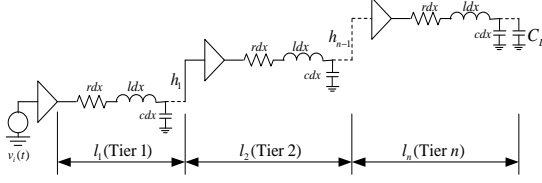


Fig. 4 Equivalent circuit of driver-interconnect-load structure of inter-tier interconnect in 3D IC

The total delay D of such an interconnect is the sum of all the segments delay d_{l_i} and vias delay d_{h_i} , which can be expressed as:

$$D = \sum_i^n d_{l_i} + \sum_i^{n-1} d_{h_i} \quad (2)$$

Since each tier i ($i = 1, \dots, n$) may be of different impedance characteristic, we can alter the position of each via to minimize the total delay of the interconnect. The length of segments l_i should satisfy [2]:

$$l_{\min_i} \leq l_i \leq L - \sum_{j=1, j \neq i}^{n-1} l_{\min_j} - \sum_j^{n-1} h_j \quad (3)$$

Here l_{\min_i} is the minimum permitted length of segment in Tier i , and it is determined by design rule or design constraints.

3.2 Impedance Matching

If a signal is traveling down an interconnect and the instantaneous impedance the signal encounters at each step ever changes, some of the signal will be reflected and the remaining distorted signal will continue down the line. These reflections and distortions lead to degradation in signal quality and cause signal integrity issues, such as ring and undershoot [6]. Therefore, it is necessary to consider impedance matching in the design of signal propagation. In this section, we consider the signal reflection resulted from the impedance mismatching as the our second goal (remember our first goal is to minimize the total delay of interconnects).

Since signal reflections occur whenever the instantaneous impedance changes, we consider the issue of impedance matching by redundant via insertion when we perform via placement.

According to the transmission line theory, the amount of signal that is reflected depends on the magnitude of the change in the instantaneous impedance. The reflection coefficient ρ is used to measure the amount of reflected signal and it is expressed by following Equation (4) when signal enters segment 2 from segment 1 [6]:

$$\rho = \frac{Z_2 - Z_1}{Z_2 + Z_1} \quad (4)$$

Here Z_1 is the instantaneous impedance of the segment

1 from which the signal initially enters, Z_2 is the instantaneous impedance of the segment 2 where the signal just enters.

The instantaneous impedance of wire depends on the cross section of the wire and the material properties [6], and it should be equal to the characteristic impedance of the wire for an impedance-controlled interconnect. The characteristic impedance Z_0 of transmission line with distributed R , L , C and G components can be determined by the following Equation (5) [8]:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad (5)$$

In the cases when the frequency is high enough, Equation (5) can be reduced to [8]:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \approx \sqrt{\frac{L}{C}} \quad (6)$$

Thus, based on Equation (4) and Equation (6), we can calculate the reflection coefficient ρ_i ($i = 1, \dots, n-1$) when signal enters via h_i from a segment l_i of interconnect in Tier i as:

$$\rho_i = \frac{Z_{0_{l_i}} - Z_{0_{h_i}}}{Z_{0_{l_i}} + Z_{0_{h_i}}} \quad (7)$$

Then we can minimize the reflection coefficient ρ_i using via sizing based on the idea of redundant via insertion described in Section 2.

3.3 Problem Summarization and Optimization

Based on the above analysis, we summarize our problem as follows.

Given a total length of L for inter-tier interconnect through n tiers and the permitted maximum/minimum via size $V_{via-max}/V_{via-min}$ (the height of via is fixed and can not be changed), to find a proper size and position of each via ($n-1$) to minimize the total delay D of the interconnect and the reflection coefficient of each tier ρ_i :

Minimize

$$D = \sum_i^n d_{l_i} + \sum_i^{n-1} d_{h_i}$$

$$\rho_i = \frac{Z_{0_{l_i}} - Z_{0_{h_i}}}{Z_{0_{l_i}} + Z_{0_{h_i}}}, i = 1, \dots, n-1$$

subject to

$$\sum_{i=1}^n l_i + \sum_{i=1}^{n-1} l_i = L$$

$$l_{\min_i} \leq l_i \leq L - \sum_{j=1, j \neq i}^{n-1} l_{\min_j} - \sum_j^{n-1} h_j$$

$$V_{via-min} \leq V_{via_{h,i}} \leq V_{via-max}, i = 1, \dots, n-1$$

This is a multi-objective optimization problem, and it can be decomposed into two equivalent sub-optimization problems: via-sizing and vias insertion/placement. Based on an iteration procedure, we can solve this optimization problem.

We first set the size of each via to an initial value (for example, the permitted minimum size) and perform vias insertion/placement to minimize the total delay with the consideration of non-uniform impedance. For each vias insertion/placement corresponding to the minimum total delay, we then alter the size of each via to minimize reflection coefficient ρ_i ($i = 1, \dots, n - 1$). Since the total delay of the interconnect may be changed for each new vias size, we need to verify the total delay based on the new vias size. If a greater total delay is obtained, a new vias insertion/placement will be conducted again based on the new vias size. Based on the above iteration, we will finally find the minimum total delay for the interconnect and the corresponding reflection coefficient. We summarize the above procedure as following algorithm:

1. Initialize $V_{via_i} = V_{via-\min}$, $i = 1, \dots, n - 1$
2. Perform vias insertion/placement to minimize the total delay of whole interconnect
3. Repeat
 - a. Resize each via V_{via_i} ($V_{via_i} \leq V_{via-\max}$), compute and find the minimum ρ_i , $i = 1, \dots, n - 1$
 - b. Check the total delay
 - c. Perform vias insertion/placement for a greater total delay
 - d. Update vias' geometric size, position and the total delay of interconnect
4. Return the optimum results

Since the expressions of segment and via delay can not be expressed as a simple linear form, the Lagrangian relaxation can be utilized to pre-process them in order to obtain the solution more efficiently.

4. Simulation Methodology and Setup

To verify our approach proposed in this paper, we conducted some simulations. The simulation methodologies are described in this section.

4.1 Delay Calculation

Since we adopt a distributed RLC interconnect structure to model the interconnects in 3D ICs, we calculate the delay of interconnects based on a distributed RLC model proposed in [7]. According to [7], an empirical RLC delay equation based on curve-fitting was derived as:

$$t_{50\%} = (e^{-2.9\zeta^{1.35}} + 1.48\zeta) / \varpi_n \quad (8)$$

where

$$\varpi_n = \frac{1}{\sqrt{L_{int}(C_{int} + C_L)}} \quad (9)$$

$$\zeta = \frac{R_{int}}{2} \sqrt{\frac{C_{int}}{L_{int}}} \frac{R_T + C_T + R_T C_T + 0.5}{\sqrt{1 + C_T}} \quad (10)$$

$$R_T = R_s / R_{int} \quad (11)$$

$$C_T = C_L / C_{int} \quad (12)$$

here C_L is the load capacitance, R_{int} , C_{int} and L_{int} are the total line resistance, capacitance, and inductance, respectively, and R_s is the output resistance of driver (inverter).

Remark 1: The objective function D (Equation (2)) based on the delay Equation (8) (Equation (1)) is convex under constraint L .

Proof. First we observe that the delay of a wire can be considered as the function of its length, since the electrical parameters in Equation (8) like interconnect resistance (R_{int}), capacitance (C_{int}) and inductance (L_{int}) can be written as the function of interconnect length. Also, the ζ (Equation (10)) is non-negative under interconnect length constraint L (Equation (1)). Furthermore, since the function $f(x) = e^x$ is strictly convex in the interval $(-\infty, +\infty)$, so the monomial $e^{-2.9\zeta^{1.35}}$ is also convex. Additionally, it is notable that ϖ_n (Equation (9)) is non-decreasing function. According to [9], the delay equation (8) is hence convex. Similarly, we can know that the objective function D (Equation (2)) is also convex. \square

According to Remark 1, the objective function D has a single global minimum, which implies that our approach is practical under the RLC delay model.

It is notable that other delay models/equations can also be used in our approach. For example, we can prove that the objective function D with the traditional or fitted Elmore delay model is also convex. Notice that the objective function D expressed by Equation (2) is of a separable non-linear form, so it can also be transformed into a form solved by geometric programming tools efficiently.

4.2 Parasitic Extraction of Vias

Since we intend to minimize the reflection coefficient of different segments and the delay resulted from vias, it is necessary to calculate the parasitic parameters such as resistance, capacitance and inductance of vias. Nevertheless, it is impractical to extract accurate parasitic parameters with existing equations rapidly. In this paper, we apply the following methods to extract the resistance, capacitance and inductance of vias respectively.

The vias' resistance R_{via} can be simply evaluated as $R_{via} = r \cdot l / w$, where r , l and w are the resistance of unit length interconnect, the interconnect length and interconnect width, respectively.

For the evaluation of capacitance, we adopt a

quasi-3D on-chip capacitance model proposed in [10] to calculate interconnect capacitance. Since the detailed layout of vias is unknown, we can only calculate the self component of vias' capacitance, i.e., the capacitance of vias coupling to substrate.

Finally, we need to calculate the inductance used in the RLC delay model. Notice that it is usually formidable to extract the accurate interconnect inductance, because the current return paths are very complicated in a real chip. To make the evaluation of interconnect inductance tractable, we adopt here the formulas proposed in [11] to extract the inductance. Similar to the calculation of capacitance, the mutual inductance between one via and the others can not be computed without the detail layout.

Notice again that we use those parasitic extraction equations described here only for enabling the simulation of our approach, the accurate parasitic parameters can be extracted accurately with 3D field solver by EDA tools when detailed layouts of chip are almost determined.

4.3 Parameters Settings

Our simulation are conducted based on a 65nm CMOS technology under the Berkeley Predictive Technology Model (BPTM) [12]. We assume that a 50X size inverter is inserted into each segment of tier. The output resistance R_s and input capacitance of inverter are calculated with SPICE. The load capacitance C_L is $0.1pF$.

To mimic the different impedance characteristics of each tier in 3D ICs, the range of resistance, capacitance of interconnect are the same as the ranges proposed in [2] and they are extracted for several interconnect structures using a commercial impedance extraction tool. The resistance of segments ranges from $5\Omega/mm$ to $25\Omega/mm$, and the capacitance of segments ranges from $100fF/mm$ to $300fF/mm$. The inductance ranges from $650pH/mm$ to $17.9nH/mm$, where the minimum value is the same as that in [7] and the maximum value is the same as that used in [13]. The minimum length routed in each tier is set as $20\mu m$.

We assume that the height of via that connects two tier ranges from $20\mu m$ to $40\mu m$. Depending upon the size of via, the resistance, capacitance and inductance of via are calculated using the methods/equations mentioned in Section 4.2. The cross-section of via is supposed to be rectangle and its size ranges from $100nm \times 100nm$ to $300nm \times 600nm$.

We tested 3 inter-tier interconnects whose length are $1.5mm$, $2.5mm$ and $3.5mm$, respectively. These interconnects are supposed to be routed in 3D ICs with 4, 6, 8 and 10 tiers. We also assume that the tiers are bonded with copper metal pads.

5. Simulation Results

We accomplished the simulations with MATLAB. In this section, we first show the delay improvement based on our approach, then we explore the effects of impedance matching on reflection coefficient.

5.1 Delay Results

The detailed results of optimum delay (D_{opt}) are listed in Table 1, the delay results (D_{equ}) for the interconnect divided equally by vias are also listed in Table 1 in order to compare with the optimum ones.

Table 1 Delay results of interconnects

Tiers (n)	Length of wires (L)	D_{equ} (ps)	D_{opt} (ps)	Delay Improvement (%)
4	1.5mm	32.87	29.63	9.86
	2.5mm	40.36	37.47	7.16
	3.5mm	52.54	48.79	7.14
6	1.5mm	34.74	30.42	12.44
	2.5mm	43.41	39.82	8.27
	3.5mm	54.96	51.87	5.62
8	1.5mm	35.79	31.45	12.13
	2.5mm	46.75	44.08	5.71
	3.5mm	56.81	53.43	5.95
10	1.5mm	38.26	32.22	15.79
	2.5mm	49.34	45.18	8.43
	3.5mm	57.49	54.17	5.77
Average				8.7%

The results in Table 1 indicate that the total delay for all 3 inter-tier interconnects based on our approach are smaller than that of interconnects divided by vias equally, where the maximum delay improvement is as high as about 16% for a $1.5mm$ wire routed in a 10-tiers 3D IC. We can also see from Table 1 that an average delay improvement of 8.7% is obtained for all 3 interconnects, compared to the instance where interconnects is divided by vias equally.

A further observation to results in Table 1 reveals that the relatively short interconnects routed in many tiers have greater delay improvement than long ones routed in few tiers. It means that the relatively short interconnects are more sensitive to different impedance characteristics of tiers in 3D ICs than long ones.

It is notable that delay improvement in our approach is smaller than that in [2]. The reason is that a distributed RLC delay model is adopted and a inverter is inserted into the segments in each tier in our simulation to imitate the actual scenario, so the overall delay of interconnect has been significantly reduced, thus leave a small space for further delay reduction.

5.2 Improvement of reflection coefficient

To explore the effects of impedance matching based on

our approach, we calculate the average reflection coefficient of all 3 interconnects for both optimum method (ρ_{opt}) proposed in this paper and equal-space vias placement (ρ_{equ}). The corresponding results are listed in Table 2.

Table 2 Results of reflection coefficient

Tiers (n)	Length of wire (L)	ρ_{equ}	ρ_{opt}	Improvement (%)
4	1.5mm	0.11	0.09	18.18
	2.5mm	0.14	0.12	14.29
	3.5mm	0.13	0.11	15.38
6	1.5mm	0.14	0.09	35.71
	2.5mm	0.21	0.13	38.1
	3.5mm	0.21	0.14	33.33
8	1.5mm	0.14	0.13	7.14
	2.5mm	0.24	0.21	12.5
	3.5mm	0.23	0.16	30.43
10	1.5mm	0.18	0.12	33.33
	2.5mm	0.22	0.14	36.36
	3.5mm	0.24	0.15	37.5
Average				26

In the Table 2, a significant difference can be observed in the reflection coefficient, depending on whether the impedance matching is considered or not. The maximum improvement is up to 37% for 3.5mm wires routed in a 10-tiers 3D IC; and the average improvement of reflection coefficient for all 3 interconnects is as high as about 26%. The low relatively improvement for the 1.5mm wire routed in a 8-tiers 3D IC appears (the absolute improvement of reflection coefficient is only 0.01). It is likely that our approach can not handle them to obtain a small reflection coefficient, due to a big difference in the characteristic impedance between segments in the wire and vias. Nevertheless, we obtained a considerable average improvement of reflection coefficient in the overall cases.

Generally, the results in this section reveal that our approach is valid for via insertion/placement in 3D ICS. It can not only decrease the total delay of inter-tier interconnects but also reduce the signal reflection and thus improve the signal integrity.

Notice that we calculate the characteristic impedance Z_0 of all segments and vias approximately with Equation (6) here. An accurate calculation of characteristic impedance of segments and vias can be achieved by some EDA tools with field solver. Other accurate characteristic impedance formulas can also be integrated into our approach without affecting the validity of our approach.

6. Conclusions

Based on the extended idea of redundant via insertion in 3D ICS, we propose an approach that supports via placement and impedance matching simultaneously when routing wires and placing vias. Simulation results

demonstrate that our approach is valid and show a significant improvement in reflection coefficient. Thus, our approach is promising to improve the design of 3D ICS, especially in post routing stage of such design.

We expect that the idea of redundant via insertion/placement can also be exploited in power and clock distribution networks to enhance their performance in the presence of process variations [14], [15] in 3D ICS. In addition, this idea can also be applied to thermal via insertion for improving the stability of whole system.

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